Design and Analysis of Reduced Test Power in Scan Based Design

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***Abstract*-Low power VLSI testing is indispensible in switching components and number of hardware/software-based techniques has been still developed to minimize the dynamic power dissipation. In earlier days, primary concerns of VLSI design were focused in area, performance, cost and reliability. But in current years, the design constraints have begun to change because of increasing low power testing. XOR network based techniques have been widely implemented for large scan chain design owing to its high compression ratio. The proposed work explores the reduction of scan power by reducing the number of switching in the XOR network. This work is also associated with Travelling Salesman problem to find out the least number of switching.**

Keyword- XOR network, Scan power, Switching, Travelling Salesman problem, Scan chain.

I.INTRODUCTION

Modern VLSI testing system needs large number of constraints which must be calculated. Testing also requires monitoring of results; and a comparison is made with a designed specification and displayed in an easily understandable format. In case of complex circuits it is time consuming and difficult to perform manually, the test and measurement using the conservative, isolated pieces of test equipments. To match with the difficulties of testing, Automatic Test Equipment (ATE) is used to provide the remarkable suppleness by allowing various kinds of components to be monitored without any alterations in the test hardware. Software alterations are programmable according to the tester types for containing various kinds of devices. It enables VLSI testing at high speed even though at very high economic- cost. Scan chain is one of technique used in Design For Test (DFT).

Scan chain provide testing easier in a simple way to set and observe flip-flop in Integrated Circuits (IC). This scan chain has Scan in and Scan out values. In a scan chain usually each input drives only one chain and scan out one as well. When the scan enable pin is asserted the flip-flop in the design is connected to the shift register. In a full scan design ATE is particularly simple. A Multi Input Signature Register (MISR) is one of the methods of examining all middle outcomes of set of registers available at the end of an instruction stream even if the final value does not depend on the value of all intermediate results, using a single MISR to generate the signature of all updates to many multi design registers. The expected final MISR value is compared by the actual final MISR value (Signature).

This paper concentrates on finding the least number of transititions by comparing all the outputs. The method called Travelling Salesman Problem (TSP) is used to find the path with least number of switching in the output patterns.

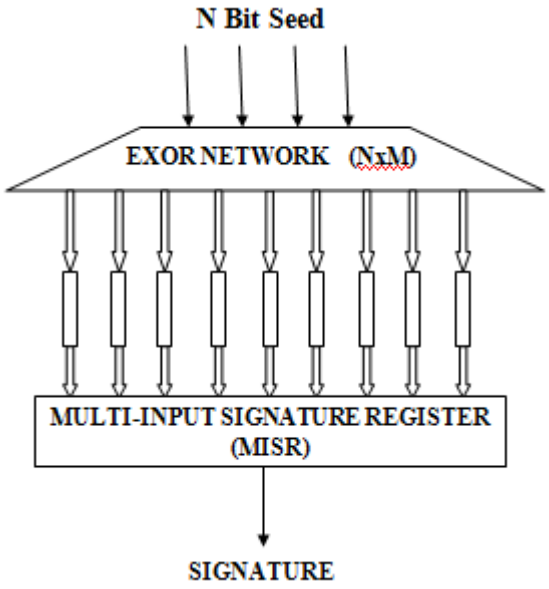

Figure I: Scan test design with EXOR network.

The representation of the scan test design with EXOR network is shown in figure 1. For every scan cycle the ATE feeds N-bit as its input to the EXOR network. All the bits from the EXOR network are produced in parallel manner and these values are given as the scan-in values. So to minimize the count of hardware required for compressing a multiple bit stream, MISR can be used. The examined value at the end of the original scan chain is compact in analogous using an EXOR which depends the MISR.

II.RELATED WORK

The arithmetical and algorithmic frame work for power aware test data has been proposed in paper [1]. This method has no impact on hardware overhead over traditional linear compression schemes. This technique delivers some amount of scan power reduction by means of Gauss Jordan Elimination method. The relationship between the signal probabilities is explored in paper [2]. High compression could be raised by the partition of scan flip-flops in which the data's were skewed. High compression can be achieved by portioning the scan cells. The work proposed in Paper [3] is reduction of power in test compression environment. The linear system is altered based on Gauss- Jordan Elimination for identifying the data with the specified bits.

This work mainly targeted on satisfying an X variable in the place of particular X-bit in all process. The selective encoding method in paper [4] decrease the test data capacity and operational time for scan testing for Intellectual Property (IP) cores. For every clock cycle the slices of data's are fed to the scan chain. A power conscious linear data compression schemes has been implemented in paper [5], which exploit the elasticity in the seed space and also find the best suited seed for minimizing power during compression technique. A new scan architecture in [6] named as reconfigured scan results with low test volume and cost. Many schemes have been proposed for linear decompression [7] proposed methods for improving the compression schemes are scan inversion and reconfiguration of the decompressor.

The remainder of this paper consist of section 3 has the work proposed for reducing the switching. Section 4 has the identification of power optimal seeds. A brief review of branch and bound algorithm in Travelling Salesman Problem (TSP) is presented in section 5. Finally the result is discussed in section 6. Some samples of the shortest path and distance is shown.

III.PROPOSED WORK

In this paper the input patterns of all possible 4 bit values are fed into the XOR network which has the inputs X0,X1,X2,X3 and after giving the values it performs the XOR operation and gives the output in nine numbers namely Y0,Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8. All these results are tabulated by representing in a matrix and comparison is made for all the results. Then by using Travelling salesman Problem find the shortest path and calculate its minimum distance. This is one of the ways of reducing the switching and minimizes the power.

A. Power Optimal Seed Identification

The proposed XOR is given as,

Let X0, X1, X2, X3 be the inputs

Let Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 are the inputs

Y0 can be obtained from X0 XOR X1 XOR X2;

Y1 can be obtained from X1 XOR X2;

Y2 can be obtained from X0 XOR X2;

Y3 can be obtained from X0 XOR X1 XOR X3;

Y4 can be obtained from X1 XOR X3;

Y5 can be obtained from X1 XOR X2 XOR X3;

Y6 can be obtained from X2 XOR X3;

Y7 can be obtained from X0 XOR X2 XOR X3;

Y8 can be obtained from X0 XOR X3.

Thus the EXOR is designed with 4 inputs and 9 outputs, considering only the necessary combinational values from all four input combinations, in this way the EXOR is designed. Here all the possible 4 bit decimal values numbering from zero to fifteen are given as its inputs. The inputs are represented in binary values. Thus by performing EXOR operation for each sixteen inputs the outputs are obtained.

B. Algorithmic Framework

After getting all the outputs, a comparison is made for all the sixteen outputs with all other outputs based on the number of switching. The switching numbers are tabulated and represented in a matrix. And thus we get 16x16 matrixes i.e. a symmetric matrix is obtained. To reduce the number of switching and minimize the power a shortest path is found out based on the distance. By introducing Travelling Salesman Problem, solution for shortest path is found.

C. Travelling Salesperson Problem (TSP)

TSP is nothing but a route that passes through each city based on the minimum distance exactly once and returns to its starting node. Since our result has 16x16 matrix such that it has TSP cannot be used to solve. So in order to get an optimal solution we go for an Optimal Algorithm or Travelling Salesman Heuristics Algorithm and solve this problem to find the optimal path and distance. In Travelling Salesman Heuristics there is an algorithm called branch and bound, explores all the constraints.

The constraints are of two types the first is the upper bound which is the minimum possible values of the solution secondly the upper bound which has the maximum possible values of the solution. Every task is split into sub-tasks. The sub-tasks are extended in anticipation of a solution as long as its cost does not go above the boundaries. The ultimate goal is to solve TSP by solving a few sub problems as possible

D. Branch and Bound Algorithm

In backtracking algorithm, we give preference to downwards and search with prune to negotiate the condition space. Better performance can be intended for solving various tasks using breadth-first search algorithm with pruning. This approach is termed as branch and bound technique. The advantage of this kind of searching is, a node which was refereed “potential” when it is positioned in a queue may no not be “potential” at the time of removal. If it may be a “potential”, it is eliminated and its children are also omitted for further testing process. The demonstration of branch and bound algorithm can be done with two examples.

In case 1we reconsider the instance of knapsack problem and modify the backtracking technique used before to perform breath-first search algorithm. In case 2 tree traversal of state space to find a key to an instance of the Traveling Salesperson Problem (TSP).

IV. EXPERIMENTAL RESULT

Some samples of the shortest path and minimum distance which is found out by using branch and bound algorithm in Travelling Salesman Problem is shown in table 1.Thus the obtained result shows that the path starts from 3-12-2-13-0-14-9-4-10-5-8-7-6-1-15-11 is the shortest with the minimum distance of 45.

TABLE I
Samples of shortest path and distance

Shortest path	Total distance
1-15-2-3-12-7-8-5-10-4-9-6-13-0-14-11	46
12-3-2-15-1-6-7-8-9-4-10-5-11-0-13-14	50
6-1-15-2-3-12-7-8-5-10-4-11-0-13-14-9	52
4-9-6-1-15-2-3-12-7-8-5-10-13-0-14-11	46
14-0-13-2-3-12-1-6-7-8-5-10-4-9-11-15	48
7-8-5-10-13-0-14-9-4-1-15-2-3-12-11-6	47
3-12-2-13-0-14-9-4-10-5-8-7-6-1-15-11	45
2-3-12-7-8-5-10-4-9-6-1-15-0-11-13-14	51
8-5-10-4-9-6-1-15-2-3-12-7-0-13-11-14	49

The figure 2 shows the representation of number of switching obtained by using the branch and bound technique in Travelling Salesman Problem (TSP). This is one of the methods of reducing the switching in the test Patterns.

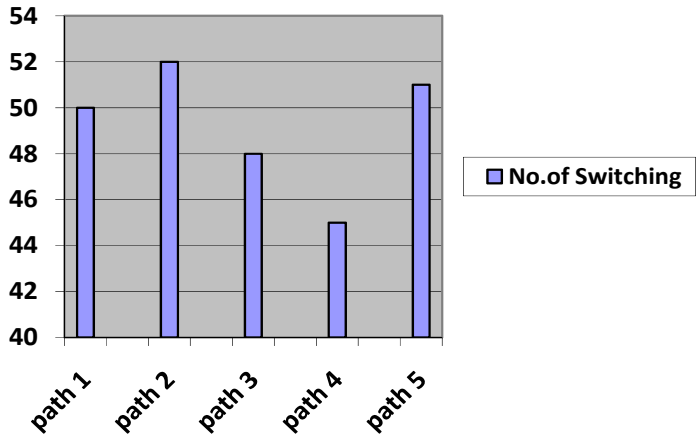

Figure II: Representation of switching

V.CONCLUSION

Thus various test patterns has been generated using EXOR network, implementing branch and bound algorithm in Travelling Salesman Problem (TSP) and found out the reduced path and distance and is verified by using MATLAB. Thus one way of reducing the power by means of finding the reduced switching has been implemented for scan based design.

VI. REFERENCES

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