

Novel Design and Implementation of Fast Fourier Transform (FFT) Using Fast Adders

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Abstract: The FFT is commonly used essential tool in digital signal processing applications. The adders used in Conventional Fast Fourier transform(FFT) are no longer appropriate for the reason that of its degraded rapidity concert. There are many dissimilar kinds of fast adders such as Carry Select Adder, Carry Save Adder and Carry Look Ahead Adder have been used for Fast Fourier Transform. However, there are always some quality loss in image and high processing time, when used in Digital image processing. The proposed FFT using the proposed fast adder is potential solution to this problem. When related to traditional equivalents, the Proposed FFT can attain less processing time, superiority loss to the digital image in our proposed FFT is insignificant.

Index Terms: Fast Fourier Transform, Signal processing, Adders.

I. INTRODUCTION

In modern Signal processing applications ,FFT plays a vital role. Fast Fourier Transform ia an algorithm for Discrete Fourier Transform. FFT which generates DFT .Figuring the fast fourier transform is indispensible assignment for many digital Signal processing applications.Many Special purpose hardware devices hav been build to do real time fast fourier transform proceesing[5].Several designs for executing the FFT using various hardwares have been discussed in the reference.

The image processing is one kind of Digital signal processing for which the image is input and the output of the processing may be eiether parameters related to digital image or an image.The processing technique includes image compression image enhancement and image reconstruction .These are some of the important parameters used in the Digital image processing Applications.

The traditional FFT which uses the adder architecture is not suitable due to its low processing speed and lack in image quality.The proposed FFT is similar to that of the conventional FFT except the Adder used in the propoed method. Here conventional adder is replaced with the proposed fast adder .By using this fast adder the FFT processing time is reduced and quqlity of image is improved.

II. EXISTING METHOD

Various numbers of research papers is focused on high processing speed and improvement in quality of image by using FFT processor.This section gives an overview of Conventional methods.In FFT processor ,the computational procedure includes enormous number of multiplications and additions. To perform the addition operation in the FFT processor conventional adders such as Carry Save Adder ,Carry Select Adder and Carry Look Ahead Adder,etc are used as shown in Fig.1. Thus FFT processor for multicarrier systems was design and implemented as given in [1]. The interstage rearrangement is done by delay commutators realized with VLSI while the arithmetic is achieved by floating point adders and multipliers.

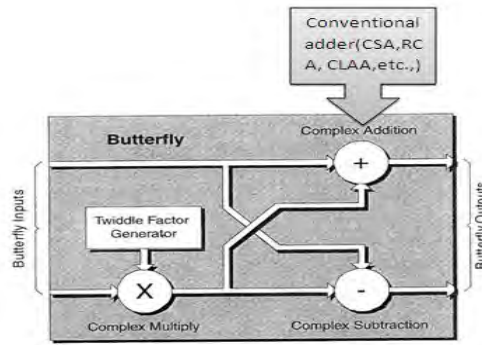


Fig.1 .Proposed Method

This paper describes the pipeline FFT operation and provides arithmetic which realizes the design[2].The Design and implementation of pipelined butterflies for radix-2 FFT using efficient adder compressors which follows the paper[3].The FFT is designed using Rapid single flux quantum adders for data flow in parallel architecture is given in paper[6].The implementation of FFT using proficient arithmetic sum of product for multiple continuous multiplication is given in paper [7].The high speed and low power FFT is implemented using the carry save addition is represented and implemented as given in paper [8]. The block diagram of Conventional FFT processor using conventional adder is given in Fig .1.

III. PROPOSED METHOD:

A.Proposed Fast Adder Architecture

In this proposed addition arithmetic,we divided the input bits into two portions accurate portion includes Most Significant Bits and the inaccurate portion includes Least Significant Bits.In the above figure the two input operands $X=1100110011000011$ (52419) and $Y=0110011011010101$ (26325), are separated similarly into Half number of bits each for the LSB and MSB portions.For higher order bits, usual addition is applied that is from LSB to MSB.For lower order bits ,it requires special addition mechanism is given in paper [4].

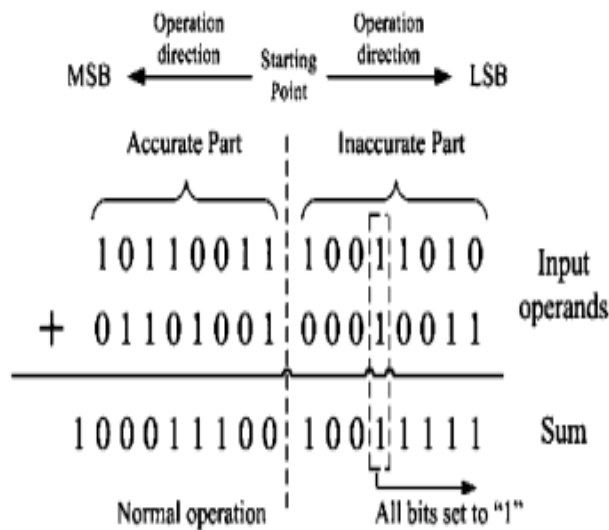


Fig .2. Proposed Addition Arithmetic

To reduce the over all fault in line for the eradication of carry chain, a distinct approach is revised and defined as follows, Patterned each single bit point from Most Significant to Least Significant Bit .If both inputs are 'Zero' or dissimilar, standard 1 bit addition is achieved and the procedure continues to next location.If both the input are '1' the examination practice clogged and since this headlong, all added bits to the Least Significant Bit are fixed to 'ONE' .The proposed arithmetic method is shown in Fig .2.

B. Hardware Implementation of Proposed fast Adder:

The process flow of the proposed work is represented in the following block diagram. This simple architecture consists of two major blocks namely accurate part and inaccurate block. The former one is implemented using the predictable adders like Carry Save Adder, Carry Select Adder and Carry Look Ahead Adder by grounding the input of carry signal. The latter one has the block with carry less addition and block to control. The working mode of the former block is determined by the control signals which can be originated by the control block. The hardware implementation of proposed adder is exposed in Fig.3.

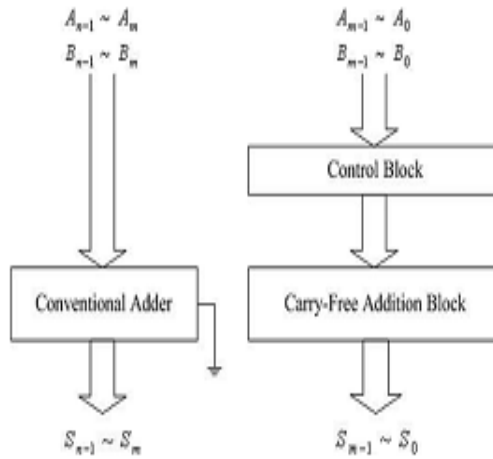


Fig. 3. Hardware Implementation of Proposed Adder

C. Proposed FFT using Proposed adder:

The proposed FFT is similar to that of the conventional FFT except the Adder used in the proposed method. Here conventional adder is replaced with the proposed fast adder

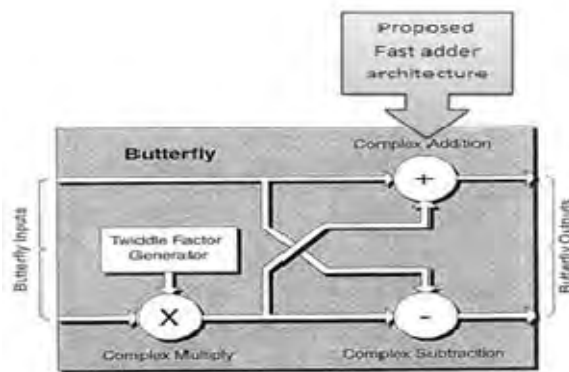


Fig .4. Proposed FFT using Proposed Adder

By using this fast adder the FFT processing time is reduced and quality of image is improved as given in the experimental results. The processing time is reduced due to very less delay time of the proposed fast adder. This gives the overview of the design of proposed FFT using Proposed Fast adder as shown in Fig.4.

IV. EXPERIMENTAL RESULTS

In Digital Signal processing the way of representing digital image is by matrix method. Thus the element in a matrix denotes the pixel of the digital image. Thus to relate the superiority of digital image it is sent through conventional FFT and Proposed FFT using Fast adders. First an Image is converted to matrix format and processed using conventional FFT and inverse FFT and then again converted to the processed image as shown in Fig.5.

Then the same image which sent first to conventional method is again converted to matrix format and processed using Proposed FFT using fast adder and their inverse is taken. After that matrix is converted to

processed image as shown in Fig.6. Thus the Fig which is produced by the proposed FFT using fast adder wave improvement in Quality and quality loss to the image negligible for the projected type and its is absolutely endured by human eyes.

The delay of the Conventional FFT using conventional adders is equated with Proposed FFT using proposed adder ,then finally from the synthesis results delay of proposed method is very less when matched with the conventional method.



Fig .5 Image Processed by Conventional FFT



Fig.6. Image Processed by Proposed FFT using Proposed Fast Adder

The Delay time compared for all the conventional adders and proposed adders is tabulated as follows and shown in table.1.

TABLE 1 Delay Comparison of Adders

Adder Types	Delay(ns)
Ripple Carry Adder	4.24
Carry save Adder	2.93
Carry Select Adder	3.65
Carry Look Ahead Adder	2.45
Proposed Adder	2.26

The Delay For all types of adders including the proposed method was analysed using Xilinx and comparison chart for same is provided in Fig.7.as Follows.

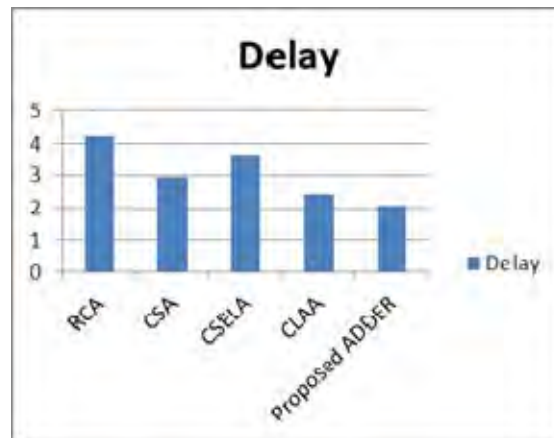


Fig .7.Delay Comparison Chart for Adders

V. CONCLUSION

To achieve high processing speed and to quality of an digital image proposed FFT using proposed adder is discussed. Various implementation of Adders for FFT is implementation methods are presented. Delay comparison for all adders are discussed and targeted to Xilinx Virtex low power 6 which produces reasonable results. Then Digital image was processed and results obtained by Matlab R2010a. The future work is related to the power optimization and area overhead reduction for same method.

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