Implementation of CIC filter for DUC/DDC

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Abstract: **In this paper a Cascaded integrated comb (CIC) filter, an optimized class of linear filters such as FIR is implemented for digital up conversion (DUC) and digital down conversion (DDC) for efficient transmission and reception in multirate system. CIC filters are often used for the purpose of reducing sampling rate (decimation) and increasing sampling rate (interpolation) . Our work is to show the efficiency of CIC filters over FIR filters in fixed point applications. Single stage CIC filter and multistage CIC filters are realized. Here multirate filter design models are developed using Xilinx system generator. Also multirate filters are further improved by cascading various CIC filter stages**.

Keywords: CIC filter, decimator, FPGA, interpolator, system generator

I INTRODUCTION

In signal processing, most frequently used procedure is to adjust sample rate frequency with respect to signal of interest. Systems dealing with different kind of sampling rates are termed as multirate system. As the need of data conversion is increasing day by day, extraction of narrow band from the wide band sources, and designing narrow band filters with wideband signals are becoming more decisive [1]. The CIC filter is formed by cascade of digital accumulator (integrator) subsequently chased by a cascade of digital differentiators (combs) in equal number. A digital switch or decimator is serviced to lower the sampling frequency of the comb signals with respect to the system sampling frequency, which is placed in between the integrators and the combs. This cascaded filter architecture is more powerful. Consider for decimation , one can get down computational complexity of narrowband low pass filter as compared with using a single stage low pass FIR, along which the filter operate at reduced clock rates, with low power and high speed applications. The reason of CIC filter more popular is because of its architecture that uses only adders, subtractors and registers. The CIC arithmetic requires no multiplication. We present CIC filter working procedure with different architectures.

After performing A/D conversion, the signal of interest could be recovered in a small frequency band compared to original frequency band transmitted, if it's so then it's necessary to filter it with a lowpass or bandpass filter to decrease the sampling rate. A narrowband filter followed by a downsampler as termed as decimator. And an upsampler ahead of a narrowband filter is termed as interpolator.

The sampling rate can be decreased up to the "Nyquist rate" which says sampling rate is twice the highest frequency that means sampling rate is higher than the bandwidth of the signal, so as to avoid aliasing.

In a band pass signal, the required frequency band for signal of interest should be within the integer band. If '***fs***' is the sampling rate, ' ***R***' is factor of decimation or downsampling then the frequency band range must be within the following,

$$k\frac{fs}{2R} < f < (k+1)\frac{fs}{2R} \quad k \in N, \tag{1}$$

If the required frequency band doesn't fall in above range then, there might be chances of aliasing due to multiple "copies" from negative frequency bands; in spite the sampling rate remain higher than the Nyquist rate In a transmitter, while D/A conversion system, increasing the sampling rate would be worthwhile, for example a typical D/A converter uses a first order sample- and -hold circuit at the output stage which produces a step output function, this could be compensated with analog function $1/sinc(x)$ compensation filter. While using more efficient solution of using an expander and additional filter to obtain the desired frequency band of interest.

II ARCHITECTURE OF CASCADED INTEGRATED COMB FILTER

(a) Primitive model of CIC :moving average filter

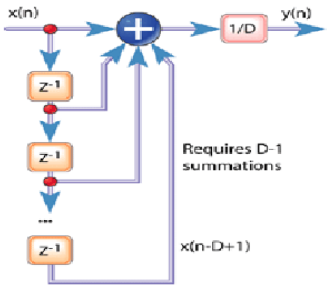


Figure 1: Moving average filter

The integrator-comb combination provides a moving average filter response at reduced cost [3]. Each integrator contributes to the CIC transfer function with a pole. Each comb section contributes with a zero of order D, where D is the frequency decimation ratio. This filter is most often used in signal processing; mainly because of its simplicity and optimal behavior for common ask like random noise reduction while retaining sharp step response. This makes it a *prime* filter for time domain encoded signal. At the same time it is *worst* filter for frequency domain encoded signals with less capacity to separate one band of frequencies from another. Moving average filter in time domain is represented as

$$y(n) = \frac{1}{D}[x(n) + x(n-1) + x(n-2) + x(n-3) + x(n-D+1)] \quad (2)$$

Its transfer function in Z- domain is expressed as

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{D}\left[1 + z^{-1} + z^{-2} + \cdots + z^{-D+1}\right] = \frac{1}{D}\sum_{n=0}^{D-1} z^{-n} \quad (3)$$

(b) Recursive running moving average

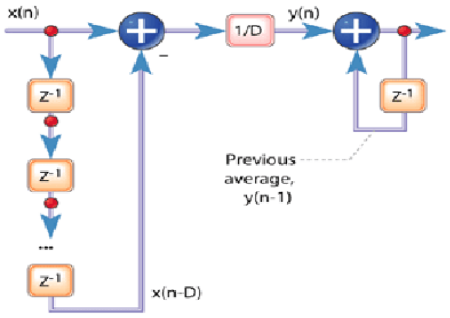


Figure 2: Recursive average sum filter

This filter is termed a recursive as it possesses *feedback* likewise each sample is holed and used to compute the next value .This can be represented by following difference equation

$$y(n) = \frac{1}{D}[x(n) - x(n-D)] + y(n-1) \quad (4)$$

Transfer function is given by

$$H(z) = \frac{1}{D}\frac{1-z^{-D}}{1-z^{-1}} \quad (5)$$

This recursive running sum average filter uses one addition, one subtraction per output sample irrespective of delay length D. This filter is used in applications where noise reduction is required through averaging [4].this recursive running filter is presented in architecture 1 of CIC filter.

(c) CIC recursive running Filter

CIC filter consists of two elementary units, integrator and comb. An integrator is a typical single –pole IIR filter of unity feedback coefficient.

$$y[n] = y[n-1] + x[n] \tag{6}$$

In Z plane it's given as

$$H_I(Z) = \frac{1}{1-Z^{-1}} \tag{7}$$

A comb filter operating at high sampling rate , 'f_s', with a rate change 'R' acts as an odd-symmetric FIR filter given below

$$y[n]=x[n]-x[n-RM] \tag{8}$$

here M is *deferential delay*. It can be any positive integer, usally considers either 1 or 2.The Z plane transfer function is given by

$$H_C(Z) = 1 - Z^{-RM} \tag{9}$$

For constructing a CIC filter, we need to cascade or bind output to input, N integrator slices along with N comb slices. The formed filter could be more simplified with a *rate changer*. If we drive the comb slice via the rate changer, then we have the following,

$$y[n] = x[n] - x[n-M] \tag{10}$$

at slower samping rate $\frac{f_s}{R}$ .By doing this we achieve three things. First constraining or holding back half of the filter thereby increasing its efficiency .Second, lessening the delay units required in comb portion. Third, the crucial arrival, the integrator and comb frame become liberated of the rate change. Now we can design CIC filter with programmable rate change.

In short, CIC decimator frame comprises cascaded *N* integrator slices clocked at f_s , chased by rate change R, followed by cascaded *N* comb slices running at $\frac{f_s}{R}$.

A CIC interpolator would comprise of cascaded *N* comb slices running at $\frac{f_s}{R}$,chased by a Zero –stuffer , and followed by cascaded *N* integrator slices at f_s .

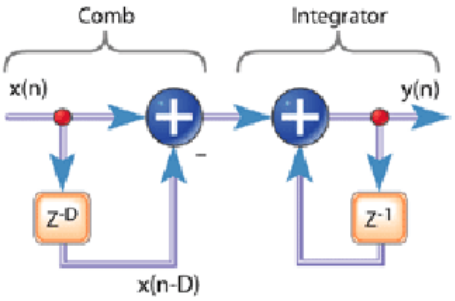


Figure 3: CIC filter

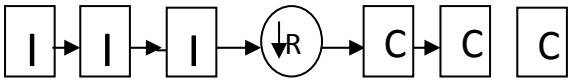
The cascaded structure of classic model without delay lines is represented in fig 3 This model condensed all delay lines of earlier model, and this is called first order CIC filter ,it consists of only adders, subtracters and registers, no multipliers unlike FIR. The feed forward section of CIC filter is termed as comb, with differential delay D, and the feedback section is called integrator. The comb section subtracts the delayed sample of input from the current samples of input, and the integrator is an accumulator. The difference equation of CIC filter is as below

$$Y(n) = x(n) - x(n-D) + y(n-1) \tag{11}$$

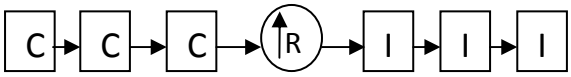
The CIC filter transfer function is defined as follows

$$H(z) = H_I^N(z)H_C^N = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} = \left(\sum_{k=0}^{RM-1} z^{-k}\right)^N \quad (12)$$

Where , z is a complex variable ,I is a basic integrator section, C is a basic comb section, M is the sampling frequency conversion factor, R is the differential delay, N is the number of stages. Here R and N be any positive integer value, system generator constrains 'R' to be either 1 or 2 as these values are not needed in most of cases. 'N' range is [1, 8]. The equation written above confirms CIC filter equivalent to cascaded N stage FIR filters along with unit coefficients. FIR filters possesses rectangular impulse response. The coefficients of FIR filter are 1 and thus symmetric, and thus CIC filter have linear phase response with constant group delay [5].



Three stage decimator



Three stage interpolator

Figure 4: Three stage CIC decimation and interpolation

III CIC FILTER ARCHITECTURES

The need of decimation or interpolation filter is for decreasing or increasing the sample rate along with keeping the pass band aliasing and spectral imaging in defined limits [5]. CIC unlike FIR for interpolation and decimation [1] satisfies all basic requirements without any multipliers, and with limited storage and making it easy to implement in economic hardware. Here in the design of decimation and interpolation, the CIC comprising integrator section and comb section in each stage of CIC functioning at high sampling rate and low sampling rate respectively

CIC filters are implemented using Xilinx System Generator and compared with its previous models; analysis of its frequency response is done for various architecture of CIC filters. If we increase the number of CIC stages, out-of-band attenuation increases. The following five architectures of CIC and response of CIC filter cascaded and decimated, four stage CIC filter, these multistage multirate CIC filters are designed with four stages of comb and integrator and with cascaded CIC filter . In CIC decimator R=8, M=1, N=4 is designed and response is as shown in figure 14. This example shows a CIC being used to implement an up sampling filter. A sinusoidal input signal is expanded by a factor of 8 and then filtered using the CIC to attenuate the spectral images.

Getting into equation (4) , its seen from the system function that the functionality of CIC filter is same as to a cascade N uniform FIR filters. Conventional form of CIC with cascade of N stages requires RM storage registers, and at least one accumulator.

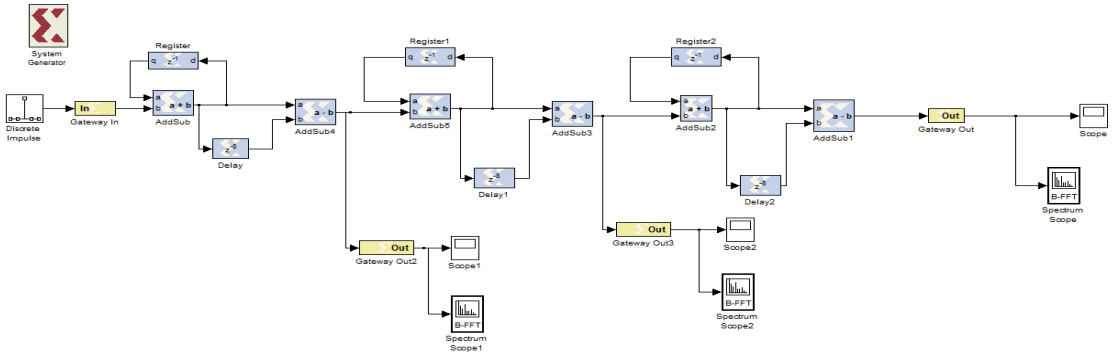


Figure 5: Recursive Average running CIC using system generator

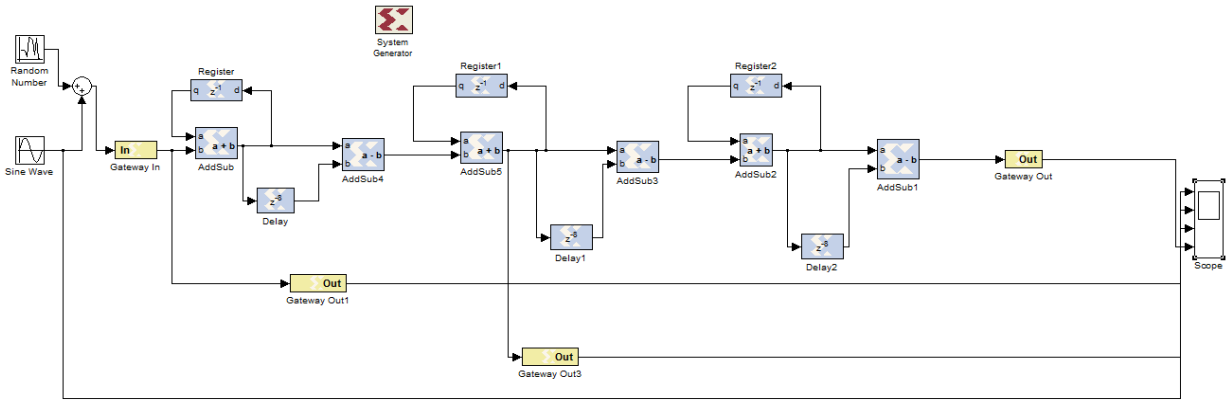


Figure 6: Architecture model 2

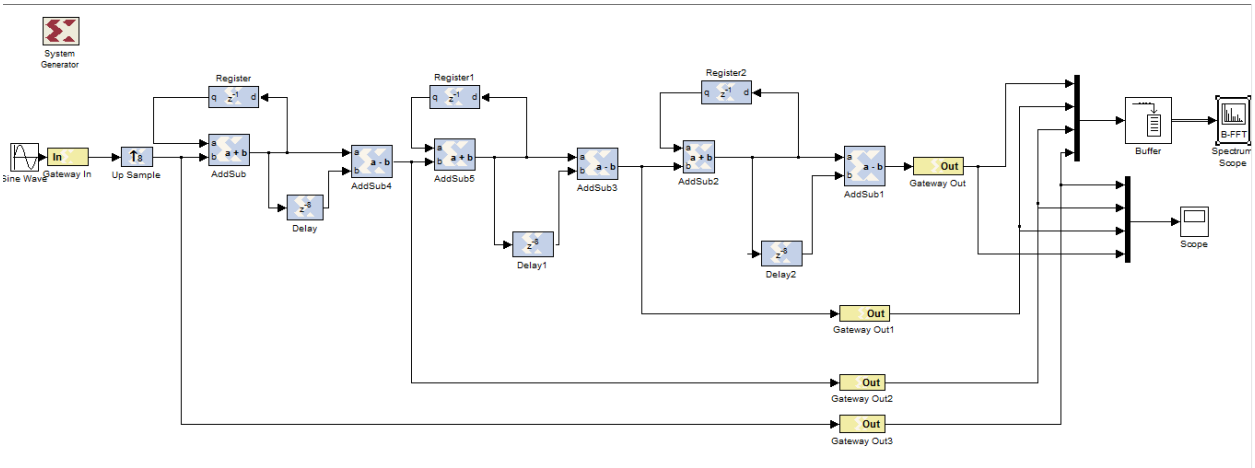


Figure 7: CIC Architecture model 3 for Interpolation

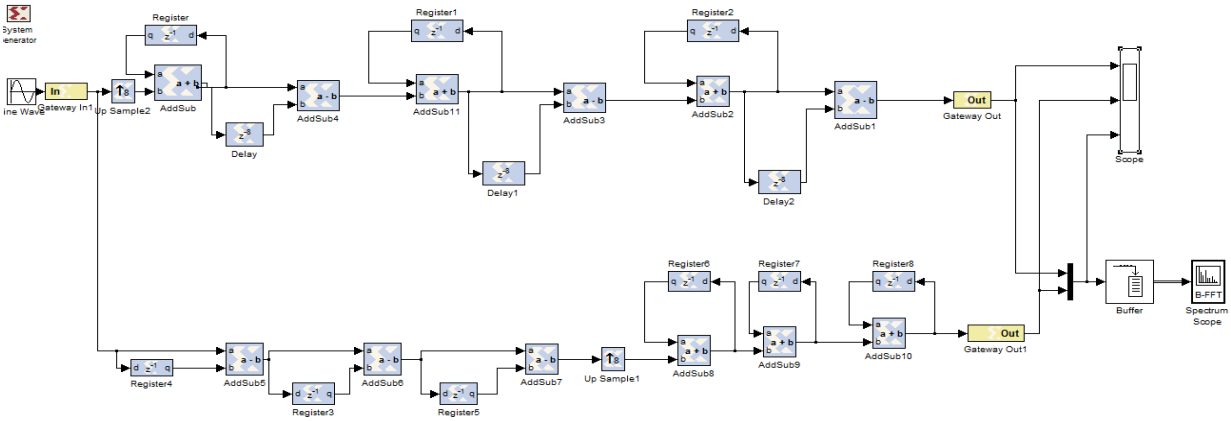


Figure 8: Architecture model 4 CIC of order 6 for interpolation

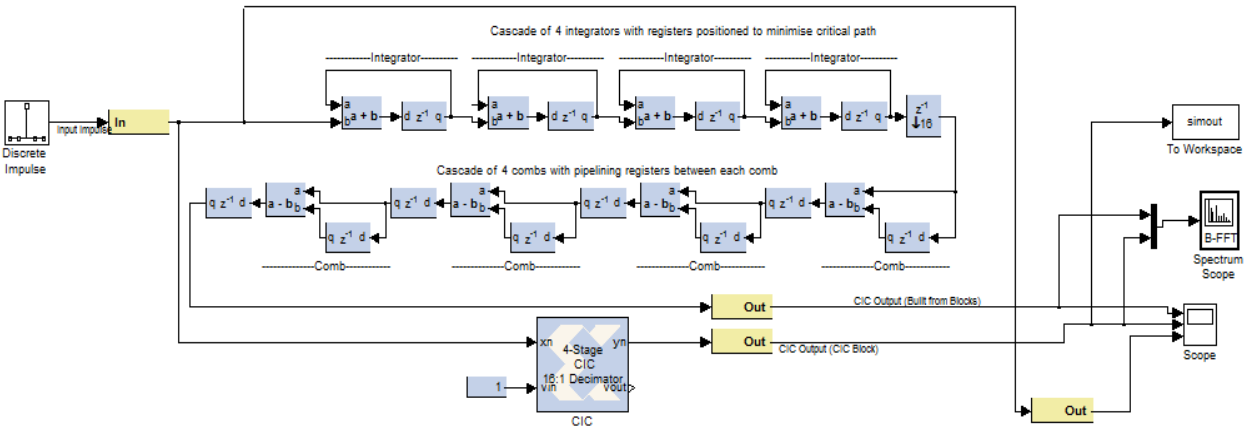


Figure 9: Decimating CIC Architecture model 5 of order 4 for decimation

IV FREQUENCY CHARACTERISTICS

CIC filter at frequency f_s is given as below

$$H(z) = H_I^N(z)H_C^N = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} = \left(\sum_{k=0}^{RM-1} z^{-k}\right)^N \tag{13}$$

The above equation reveals similarity to FIR filters, though CIC filters got accumulators (integrators) which produce infinite impulse response. Here all the coefficients of integrator slice are unity and thus symmetric, this provides a linear phase response and constant delay. The output response of the filter is as follows

$$|H(f)| = \left|\frac{\sin\pi Mf}{\sin\frac{\pi f}{R}}\right|^N \tag{14}$$

Using approximation sin$x \cong x$, *for* large values of 'R'

$$|H(f)| \approx \left|RM\frac{\sin\pi Mf}{\pi Mf}\right|^N \quad \text{for } 0 \leq f < \frac{1}{M} \tag{15}$$

We can very well analyze the response, the output spectrum constitute nulls at multiples of $f = \frac{1}{M}$. Aliasing or imaging occurs in the region around these nulls. Let f_c be the cutoff frequency of usable passband, then the regionforaliasingareat $(i - f_c) \leq f \leq (i + f_c)$ (16)

for $f \leq \frac{1}{2}$ and $i = 1,2 \ldots, \left\lfloor\frac{R}{2}\right\rfloor$. If $f_c \leq \frac{M}{2}$,then the aliasing is maximum at the low edges of the first band, to design an efficient filter we need to adjust *R*,*M*,and *N*.

With increasing number of stages or cascading the CIC we can very well control the aliasing.

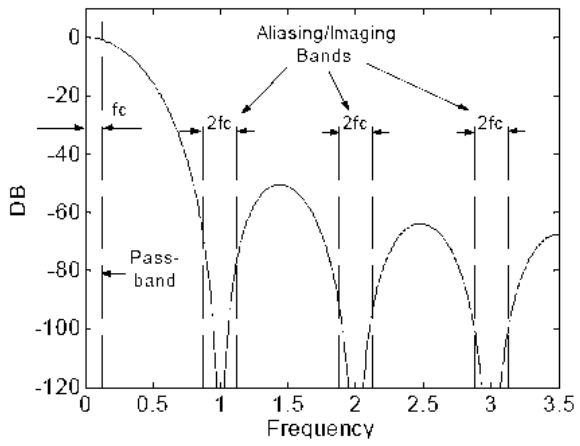


Figure 10 : frequency response for N=4,M=1,R=7 and $f_c = \frac{1}{8}$

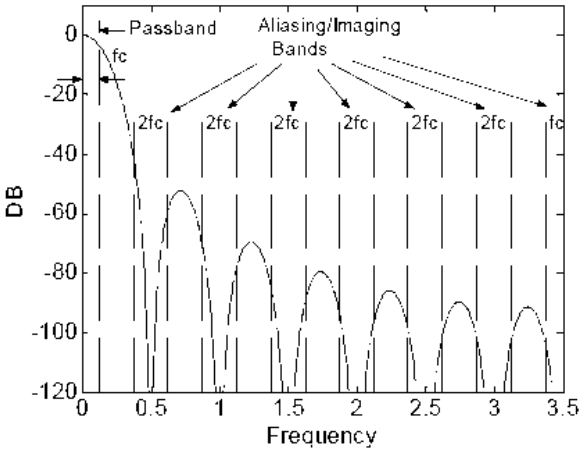


Figure 11 : frequency response for N=4,M=2,R=7 and $f_c = \frac{1}{8}$. The above figure 10 shows frequency response for a CIC filter of 4 stages N=4 , differential delay M=1and rate change factor R=7. The very next response is with literally same parameters except differential delay M=2. From the spectrum we can analyse the nulls are positioned at multiples of $f = \frac{1}{M}$.

V SIMULATION RESULTS

The architecture shown in figure 7 is CIC for interpolation; this includes parallel fixed point implementation of the CIC filter that uses 19 bit words. The input signal is noisy sine wave which we intend to clean up using CIC filter. The figure 11 shows the scope output comprising CIC output, fixed point noisy sine wave, clean floating point sine wave and the intermediate CIC output. CIC being used to implement up sampling filter, here a sinusoidal input signal is expanded by a factor of 8 and then filtered using the CIC to attenuate the spectral images. $20\,log_{10}$ FFT signal is shown in figure 12. CIC is cascaded with separate section of comb stage and integrator stage in figure 8, corresponding spectrum output signal is shown in figure 13. CIC for decimation is demonstrated in figure 9, here we have built a CIC filter with decimation factor $R = 16$ and $N = 4$ section. This filter is designed to decimate from a sampling rate of 10MHz down to 625 KHz for pass band 78.125 KHz. Non zero dB gain have been observed in FFT scope shown in fig 14. This may be compensated for using a right shift of $log2R^N = 16$ bits. There is drop in frequency response of two signals as it is decimated response.

Simulation results of various architectures are produced using Xilinx System Generator and presented here. Since CIC filters are very cheap, using them for the first stage of decimation, or the last stage of interpolation, ensures that very few DSP operations take place at the highest sampling frequency. However, usually they need to be used in conjunction with other filters (which are more expensive, but with better filtering properties). This allows the expensive filters to operate at the lowest sample rates.

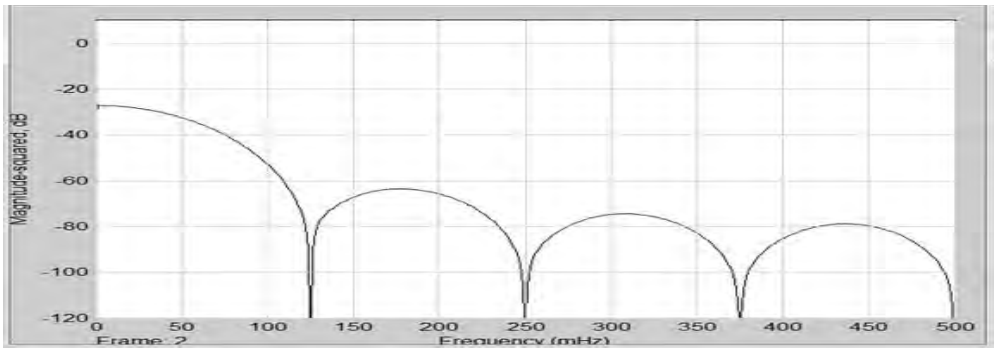


Figure 12: Frequency response of CIC filter Architecture model 1

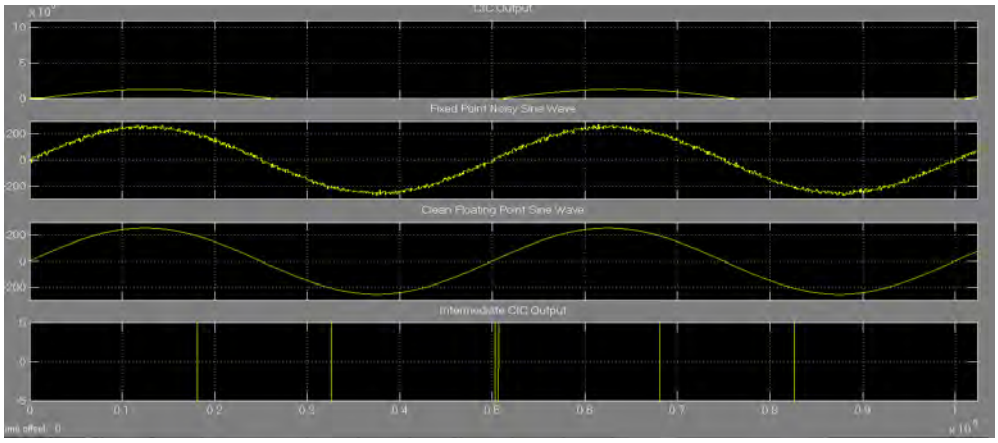


Figure 13: scope output of Architecture model 2

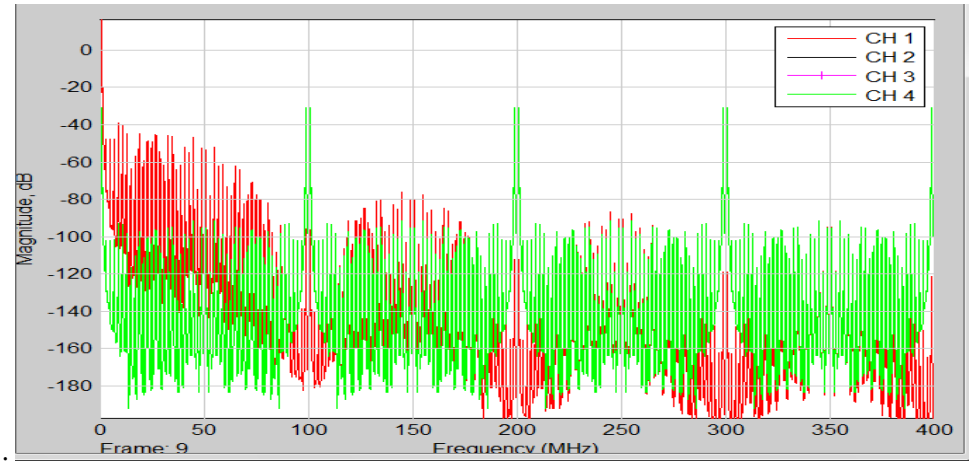


Figure 14: spectrum output of Architecture model 3

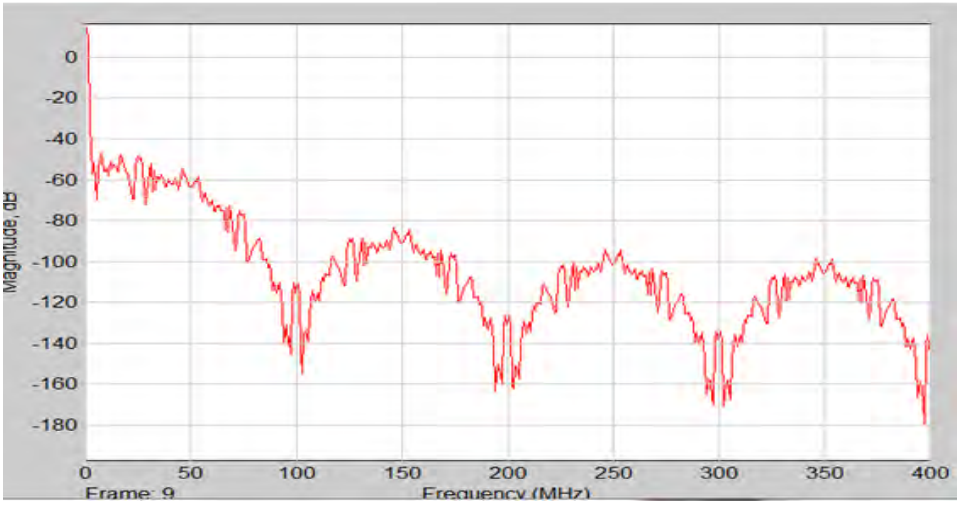


Figure 15: Frequency response of Architecture model 4

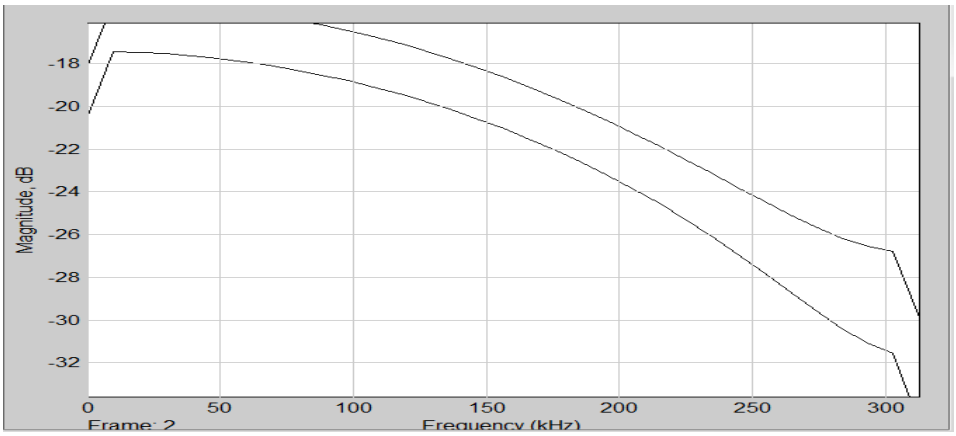


Figure 16: Output response of decimation CIC Architecture model 5

Slice logic utilization	Architecture 1 Recursive CIC	Architecture 2 Flouting point CIC	Architecture 3 Interpolation CIC order 3	Architecture 4 Interpolation CIC order 6	Architecture 5 Decimation CIC order 4
Number of Slice Registers	133	133	132	213	287
Number of Slice LUTs	171	171	148	272	526
Number of Slice Flip Flops	114	141	18	281	285
Number of bonded IOBs	68	59	78	49	40
Number of BUFG/BUFGCTRLs	1	1	1	1	1

Table 1: device utilization summery of all architecture models

VI CONCLUSION

Here CIC architecture is proposed for interpolation and decimation which turns to be better choice rather than single stage CIC filter and FIR filter for multistage multirate filtering structure and their wide responses used for decimation and interpolation These responses can be further improved by cascading more comb and integrator or by sandwiching comb and integrator. CIC filter with decimation ratio 12 ,if its cascaded with another CIC filter with decimation ratio 4 , then the overall response drastically increases by 48 times. Thus the CIC filter proves to be more efficient; it reduces power consumption and thus reduces implementation cost.

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