Low Power CMOS Digitally Controlled Oscillator

Manoj Kumar[#1], Sandeep K. Arya[#2], Sujata Pandey*[3] and Timsi[#4]

[#]Department of Electronics & Communication Engineering

Guru Jambheshwar University of Science & Technology, Hisar, 125 001, India

[*] Amity University, Noida, 201 303, India

***Abstract*- Here, two new designs of CMOS digitally controlled oscillators (DCO) for low power application have been proposed. First design has been implemented with one driving strength controlled delay cell and with two NAND gates used as inverters. The second design with one delay cell and by two NOR gates is presented. The proposed circuits have been simulated in spice with 0.35 µm (micrometer) technology at supply voltage of 3.3V. The first design shows 35-40% reduction in power consumption and second design shows 37.5-41.8% power saving as compared to conventional DCO. The frequency range of first and second design varies [3.1316 - 3.1085] GHz and [3.8112 – 3.7867] GHz respectively with the variation in control word from '000000' to '000001'. Power consumption of first and second design varies [640.3845 - 700.2977] µW and [617.6616 -6 77.3996] µW respectively.**

***Index Terms*- CMOS, current controlled oscillator (CCO), digitally controlled oscillator (DCO), phase locked loop (PLL), voltage controlled oscillator (VCO).**

I. INTRODUCTION

With wide spread CMOS technology, use of digital integrated circuits has increased many folds for reasons of size, cost, flexibility and repeatability. Phase-locked loops (PLLs) are the significant and widely used circuit's components for clock generation in many electronic computing systems such as laptops, digital signal processors and microprocessors. Traditionally analog PLL has been used for clock generation that consist of a phase detector, a loop filter, a charge pump, a voltage controlled oscillator (VCO) or current controlled oscillator (CCO) and a frequency divider circuit [1]. However analog PLL are sensitive to process parameters variations and must be redesigned with changing technology [2]. Digitally controlled clock generators are less sensitive and easier to implement.

A controlled oscillator is a key component of PLL. DCO (Digitally controlled oscillators) is a replacement of conventional VCO/CCO in the digital PLL called All-digital phase locked loop (ADPLL). DCO is the heart of ADPLL that shows higher noise immunity and robustness than the conventional PLL. However, ADPLL has major drawback of large power consumption [3] and 50% of total power is contributed by DCO [2], [3]. Since power consumption have great significance for the portable battery operated devices, power saving has become a major design concern for electronic systems. In some application, the ADPLL does not need to generate multiple frequency components but needs to operate at one particular specified frequency [4] or it may be required to generate very few frequency components. In those applications it is not desired to have a DCO with large pulling range, but the target frequency must be generated with minimum power consumption.

This paper presents improved CMOS DCO circuits with [35-42] % reduced power consumption than the conventional DCO with three stages of 12-bit driving strength controlled delay cells. Rest of paper is organized as follows: conventional DCO is described in Section II. The proposed designs of DCO have been presented Section III. Results of proposed designs and comparison with conventional DCO have been presented in Section IV. Section V concludes the work.

II. CONVENTIONAL DCO

The conventional DCO has three stages of driving strength controlled inverter cells and one AND gate for shutting down the DCO during idle mode [4]. Like VCOs or CCOs, DCOs also have frequency controlled mechanism to control the output frequency of oscillation by means of digital control word applied at the control input of DCO. Circuit generates oscillation of time period T_{DCO}, which is a function of digital control word D given by

$$T_{DCO} = f(D_{n-1}2^{n-1} + \cdots + D_1 2^1 + D_0 2^0) \quad \cdots (1)$$

A variable delay inverter is a core element of DCO and its precision directly affects the overall performance of DCO [5]. The widths of MOS transistor used in variable delay inverter are binary

weighted [6], [7], [8]. The propagation delay time of inverter is inversely proportional to equivalent MOS width [4]. With change in digital control word the equivalent width of MOS transistors varies, which changes the propagation delay time of the inverter. With fixed supply voltage, two parameters modulate the output frequency of oscillator. One is total number of delay cells connected in the closed loop and other is propagation delay time of each delay cell [9]. Circuit achieves delay variation of individual cell by changing the driving strength dynamically by means of digital control code.

Block diagram of conventional DCO is shown in Fig.1. It employs the course code as well as fine code to control the output frequency. The circuit consist of three stages of driving strength controlled inverter cells and one AND gate to enable/disable the DCO. The circuit level diagram of 12-bit driving strength controlled cell used in DCO is shown in Fig.2. The W/L ratio of MOS transistors are binary weighted which enables to achieve binary incremental delays. The sizes of the binary controlled transistors are shown in table 1. The W/L of M3 and M4 is (1/0.35) while the W/L ratio of M1 and M2 is (2.5/0.35). The complete circuit diagram of conventional DCO is shown in Fig.3. The control bit applied at the input of first two stages is used for coarse tuning while the code applied at the control input of third stage provides fine tuning.

TABLE 1
TRANSISTOR SIZES OF THE CONVENTIONAL AND PROPOSED DCO's

Transistors	M5, M11	M6, M12	M7, M13	M8. M14	M9, M15	M10, M16
(W/L) µm	2.5/0.35	5/0.35	10/0.35	20/0.35	40/0.35	80/0.35

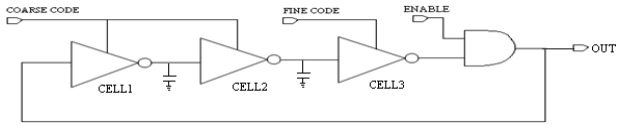


Fig.1.Conventional DCO structure

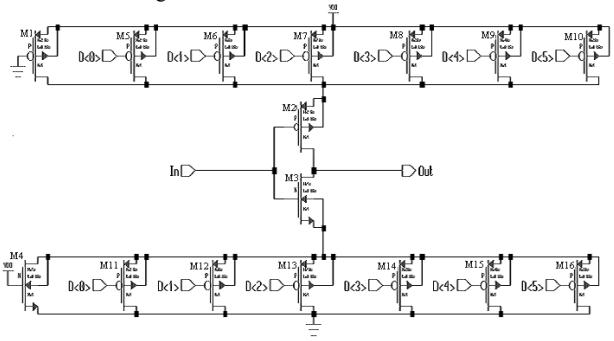


Fig.2. Driving strength controlled cell

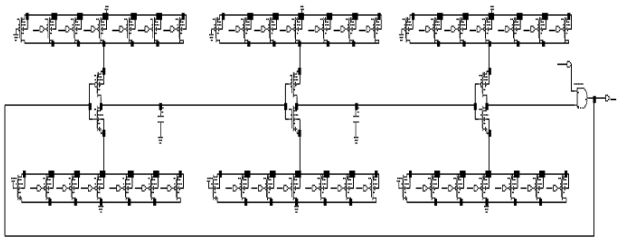


Fig.3. A 12-bit conventional DCO

III. PROPOSED DCO DESIGNS

In proposed DCO-I structure, one driving strength controlled inverter cells & two NAND gates have been used as shown in Fig.4. In the second design, inverter cell & two NOR gates have been utilized as compared to three delay cell and one AND gate in conventional DCO. In conventional DCO, control word is applied at the binary controlled input of all the three stages but in proposed DCO designs control word is applied only at the control input of first stage. Therefore, the propagation delay time of first stage i.e. driving strength controlled delay cell is only varied to control the output frequency of oscillation while propagation delay time of NAND/NOR gates remains fixed. As the number of transistors used in two proposed designs are much less than the conventional so circuit shows considerable power saving. The conventional DCO uses total 54 MOS transistors and two capacitors. On the other hand both modified circuits use only 24 MOS transistors. Due to less numbers of transistors delay time introduced by the circuit reduces and output operating frequency increases. However the numbers of frequency components that can be generated by proposed DCO are less than the conventional structure. There are applications which require particular specified frequency or need only a few frequency components. For those applications the proposed circuit shows power saving up to 40%. Fig.5 shows proposed DCO-I design using driving strength controlled delay cell and NAND gates.

Block and schematic diagram of proposed DCO-II with one delay cell and two NOR gates have been shown in Fig.6 and Fig.7.

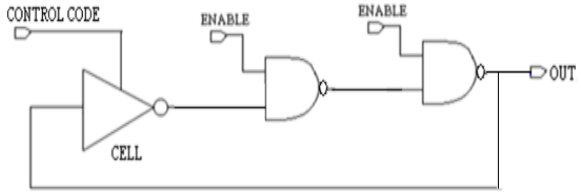


Fig. 4: Block diagram of proposed DCO-I

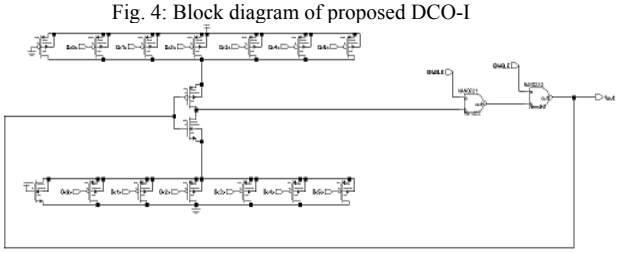


Fig.5 Schematic of proposed DCO-I

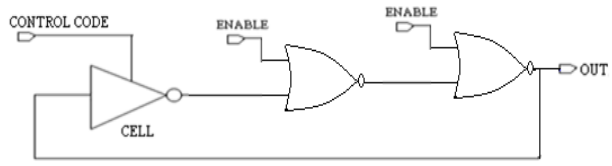


Fig.6. Block diagram of proposed DCO-II

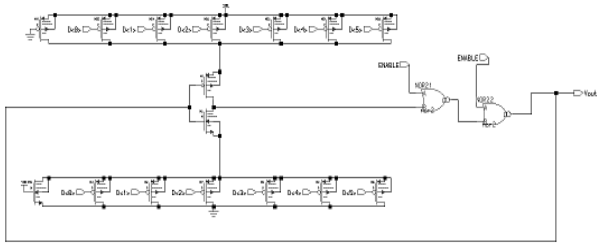


Fig.7. Schematic of proposed DCO-II

IV. RESULTS AND DISCUSSIONS

The proposed DCOs and conventional DCO have been simulated and compared using spice in 0.35 μm (micrometer) technology with supply voltage 3.3V. In order to compare the power consumption conventional and proposed design are equally sized and simulated with same input parameters.

Table 2 shows the impact of each control bit on the output frequency of three DCO structures with $(W/L)_n$=1/0.35 and $(W/L)_p$ =2.5/0.35 for NMOS and PMOS transistors. Power dissipation for three DCO structures for different combinations of control bits has been shown in Table 2. The two proposed DCO structures show significant increase in operating frequency with reduced power consumption. As compared to conventional DCO, proposed DCO-I achieves 35-40% reduction in power consumption while second DCO-II design results in 37.5-41.8% power saving. The simulation results for the conventional and proposed DCOs are shown in Fig.8, Fig.9 and Fig.10 for '000000' control word. Fig.11 shows power consumption for the three designs with variation in control word from '000000' to '000001'.

Control bits						Conventional DCO		Proposed DCO-I		Proposed DCO-II	
D<0>	**D<1>**	**D<2>**	**D<3>**	**D<4>**	**D<5>**	**Frequency (MHz)**	**Power dissipation (µW)**	**Frequency (MHz)**	**Power dissipation (µW)**	**Frequency (MHz)**	**Power dissipation (µW)**
0	0	0	0	0	0	32.444	0990.0	3131.6	640.3845	3660.4	617.661
1	0	0	0	0	0	35.879	1104.9	3121.4	679.6439	3649.5	656.810
0	1	0	0	0	0	37.154	1130.9	3112.0	688.4903	3643.6	665.646
0	0	1	0	0	0	37.995	1147.9	3112.0	694.2275	3639.4	671.379
0	0	0	1	0	0	38.469	1157.6	3112.9	697.5261	3639.3	674.677
0	0	0	0	1	0	38.773	1162.9	3111.7	699.3075	3641.3	676.458
0	0	0	0	0	1	38.909	1165.7	3108.5	700.2977	3643.1	677.399

TABLE 2

IMPACT OF CONTROL BIT ON OUTPUT FREQUENCY AND POWER DISSIPATION

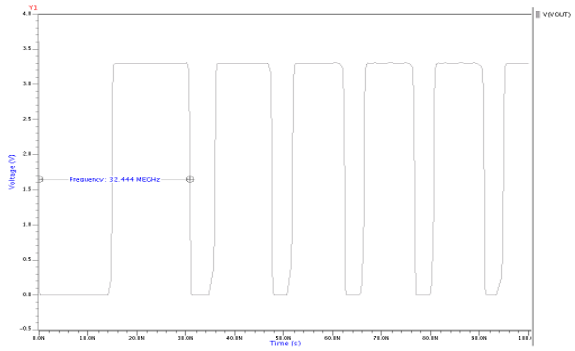


Fig.8. Output waveform for conventional DCO

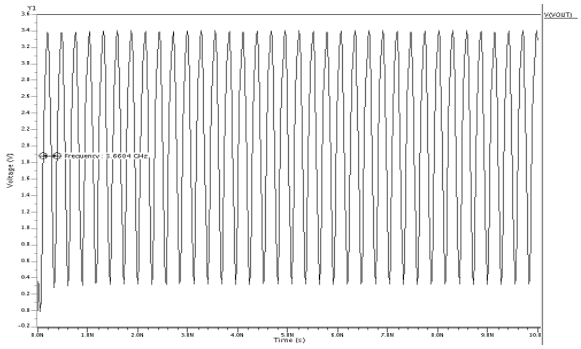


Fig.10. Output waveform for DCO-II

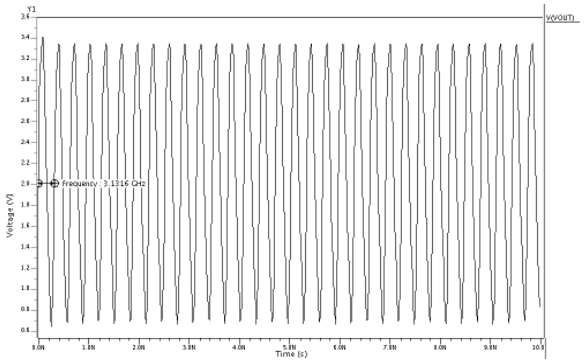
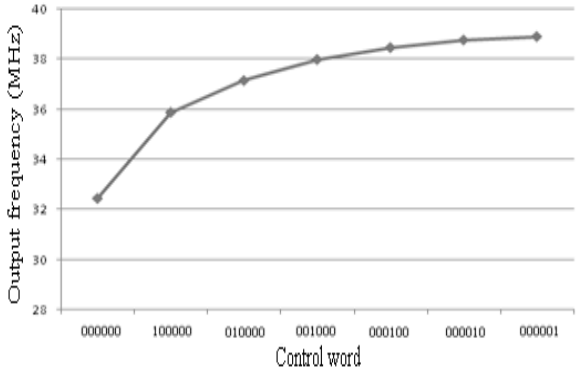


Fig.9. Output waveform for DCO-I



(a)

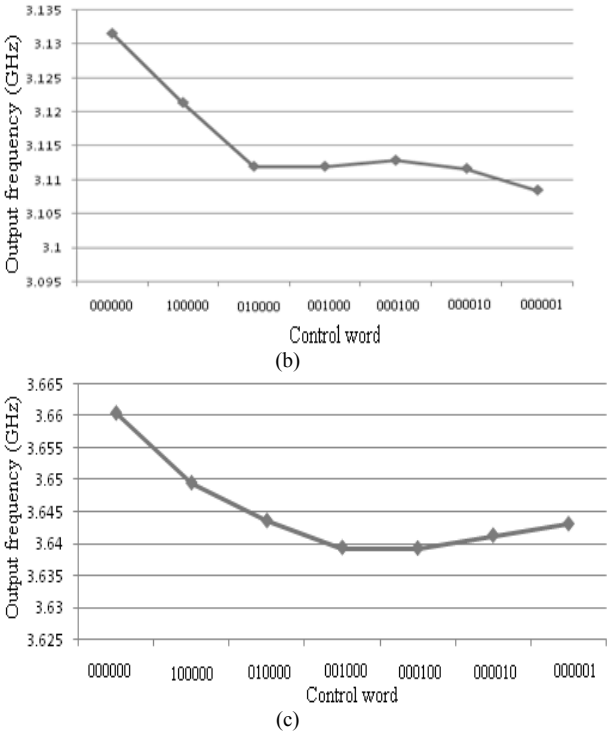


Fig.11. Frequency variation with control word (a) conventional DCO (b) DCO-I (c) DCO-II

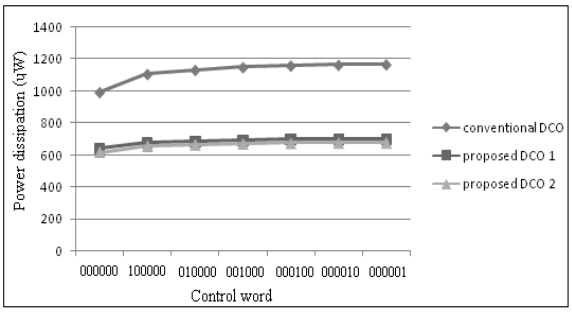


Fig.12.Power dissipation variation for the DCO structures

V. CONCLUSIONS

Two new designs for 12-bit DCO have been presented with reduced power consumption than the conventional DCO. The conventional DCO uses 54 MOS transistors where as proposed designs uses only 24 transistors. DCO implemented using driving strength controlled delay cell and NAND gates show 35-40% reduction in power consumption. The DCO implemented using driving strength controlled delay cells and NOR gates shows 37.5-41.8% power saving. The DCO-I achieves deviation in frequency from [3.1316 to 3.1085] GHz with power dissipation variation [640.3845 to 700.2977] μW. Frequency deviation for second DCO designed varies [3.6604 – 3.6431] GHz with power consumption variation [617.6616 to 677.3996] μW.

REFERENCES

[1] Jun Zhao,Yong-Bin Kim (2008), "A 12-bit digitally controlled oscillator with low power consumption and low jitter," IEEE International MWCAS 2008, pp 370-373.

[2] Thomos Olsson and Peter Nillson (2004), "A digitally controlled PLL for SoC application," IEEE J. Solid-State Circuits, vol.39, pp. 751-760.

[3] Duo Sheng, C. C. Chung, C. Y. Lee (2007), "An Ultra Low Power and Portable Digitally Controlled Oscillator for SoC applications," IEEE trans. on circuits and systems-II, vol.54, pp. 954-958.

[4] J.-J. Jong and C.-Y. Lee (2001), "A Novel Structure for the Portable Digitally Controlled Oscillator," in Proc. IEEE Int. Symp. Circuits and Systems, vol.1, pp. 272–275.

[5] M. M. Nejad and M. Sachdev (2005), "A Monotonic Digitally Controlled Delay Element," IEEE J. Solid State Circuits, vol. 40, no.11.

[6] Jim Dunning, Gerald Garcia, Jim Lundberg, and Ed Nuckolls (1995), "An all digital phase - locked loop with 50-cycle lock time suitable for high performance microprocessors," IEEE J. Solid - state Circuits, vol. 30, no.4, pp. 412-422.

[7] Jen - Shiun Chiang and Kuang -Yuan Chen(1998), "A 3.3V all digital phase locked loop with small DCO hardware and fast phase lock ," ISCAS '98, vol.3, pp.554-557.

[8] Cheong F. Chan and Oliver Choy (2001), "A low power digitally controlled oscillator," Int. J. Electronics, vol. 88, no. 4, pp. 463-466.

[9] Tzu-Chiang Chao and Wei Hwang (2006), "A 1.7mw all digital phase locked loop with new gain generator and low power DCO," IEEE International Symposium on Circuits and Systems, pp.4867-4870.