Digital frequency meter using DMA Terminal Count stop method

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Abstract-This paper presents a new wide-range speed measurement method, using the direct memory access (DMA) terminal count register(TCR). The DMA method is based on both pulse counting in the constant sampling time at terminal count stop pin of a DMA controller. The hardware configuration and algorithms for a microcontroller implementation are also presented. The proposed method is suitable in systems using microcontrollers with DMA controller and timers. Limitations and sources of errors are discussed in details. The DMA Terminal count register method is suitable for real-time speed control systems.

I. Introduction: The speed measurement can be achieved using the following methods

1. Time measurement-determines time interval between pulses[1]
2. Pulse counting-counts input pulses within sampling time[2]
3. Combined method[3]
4. Constant Elapsed Time method(CET)[4]
5. DMA Transfer method.[4][5]

When the hardware configuration of the DMA Transfer method executes a long processor instruction, it is possible that DMA acknowledge signal **(**DACK**)** is not received before the next rising edge of input pulses. Therefore, this next pulse will not be detected. In order not to lose any input pulse the counter of unperformed DMA requests is used. This can also be solved using a simple h/w configuration and less power consumption method which can be achieved using terminal count register and TC stop pin of DMA controller. The TC stop pin of DMA Controller changes its state after fixed number of DMA cycles. The numbers of pulses generated from oscillator are counted within these DMA cycles. This is proportional to the speed to be measured. A DMA controller 8257 is selected in my work because of its simple architecture, easy to understand its management and controlling operations. The 8257 can gain control on the system bus using the CPU' hold function. The DMA count for each channel and outputs a control signal to notify the peripherals that the programmed number of DMA cycles complete[6].The DMA channel that is to be programmed should always be "masked" before loading any settings. This is because the hardware might unexpectedly assert the DRQ for that channel, and the DMA might respond, even though not all of the parameters have been loaded or updated.

II. Terminal count DMA method

In this method the average number of pulses in the buffer is counted which indicates the speed of the disk or the number of pulses arrived at DRQ.The rotational speed can be calculated from the quotient $\Delta\Phi/\Delta t$. $\Delta\Phi$ is the increment of the rotational angle during the time interval Δt, where

$$\Delta\phi = Cp * 2 * \frac{\pi}{m} ------(1)$$

$$\Delta t = C_T T_c ------(2)$$

Where m is the number of encoder marks per turn, C_P is the number of encoder pulses, C_T is the number of time clocks measured, T_C is the clock pulse period,. Using **(1)** and (2) the rotational speed n can be calculated as follows:

$$n = Cp/(Ct.m * T_c) --------------(3)$$

The minimum measurable speed is

$$n_{min} = \frac{1}{T_{max}}.m$$

Where T_{max} is maximum response time.

Relative Error

In	Pulse counting	Pulse Time Measuring	CET	TCDMA
at30rpm	85%	0.025%	0.025%	0.01%
at3000rpm	0.85%	2.5%	0.05%	0.025%

Some operating conditions and characteristics are observed as follows[6].

Operating Conditions

Symbol	Parameter	Min	Max	Units
Tc	Case Temperature	-55	+125	^0C
Vcc	Digital supply voltage	4.50	5.50	V

Some DMA Characteristics in Slave mode

Read Cycle

Symbol	Parameter	Min	Max	Units
T_{AR}	Addr or CS setup to RD	0		ns
T_{RA}	Addr or CS hold fromRD	0		ns
T_{RD}	Data Access from RD	0	300	ns
T_{DF}	DB-Float Delay fromRD	20	150	ns
T_{RR}	RD Width	250		ns

Write Cycle

Symbol	Parameter	Min	Max	Units
T_{AW}	Adr Setup to WR	20		ns
T_{WA}	Ardr Hold from WR	35		ns
T_{DW}	Data setup to WR	200		ns
T_{WD}	Data Hold from WR	10		ns
T_{WW}	WR Width	175		ns

Other Timings

Symbol	Parameter	Min	Max	Units
TRSTW	Reset Pulse width	300		ns
TRSTD	Vcc Setup to Reset	500		µs
Tr	Signal Rise Time		20	ns
Tf	Signal Fall Time		20	ns
TRSTS	Reset to First I/OWR	2		

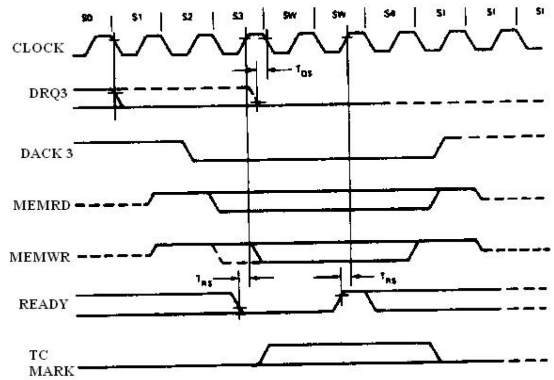
Suppose the following equation is being evaluated,

$$T_A(MIN) + T_B(MAX) \le 150ns$$

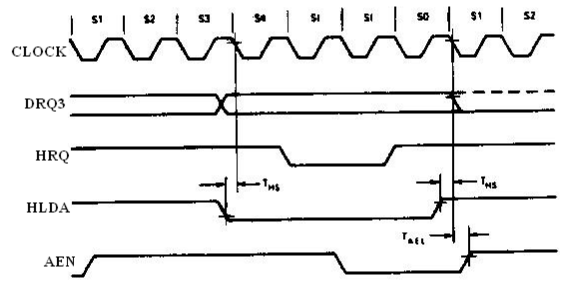
And only minimum specifications exist for T_A and T_B. If T_A (MIN) is used, and If T_A and T_B are tracking parameters, then T_B (MAX) can be taken as T_B (MIN) + 50ns.

$$T_A(MIN) + T_B(MAX) + 50ns \le 150ns$$

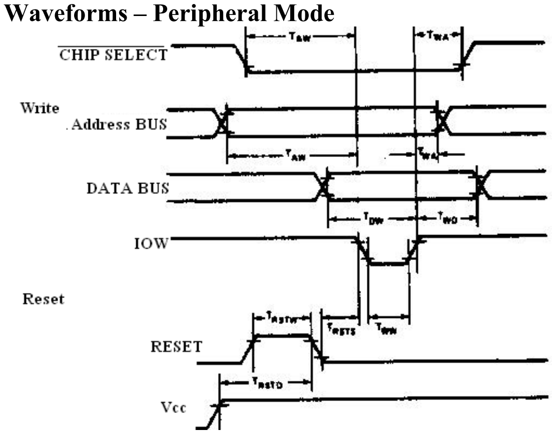
Not Ready Sequence:



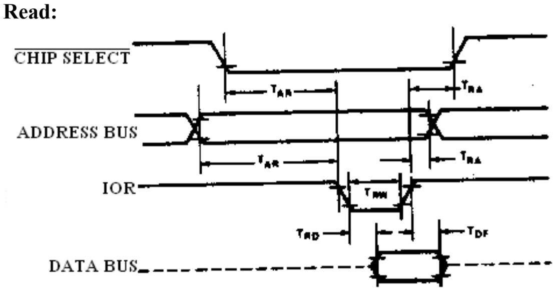
Control Over Ride:



Waveforms – Peripheral Mode



Read:



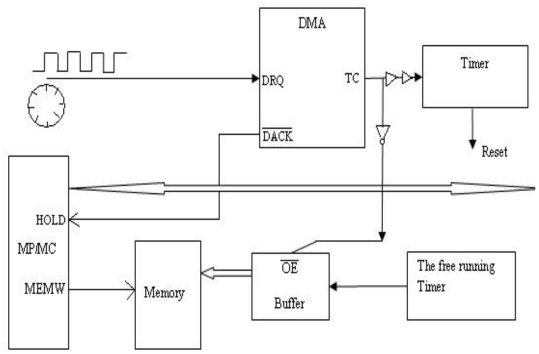
III. Terminal count DMA method features

There is limitation in speed measurement in CET method[7].Unlike the Constant elapsed time method a wide range measurements is possible as there is no time constraint as there is no necessity in disabling the capture register. Here the terminal count register is set to decide the sampling period of the TC interrupt.

Unlike the DMA method it requires less hardware and so it consumes less power as compared to wide range frequency measurement systems. More over a small algorithm can be implement which improves execution speed.

IV. Hardware Configuration:

The rising edge of the pulses from the encoder is recognized by DRQ pin of the DMA controller. As the DRQ responds to the pulses the terminal count register of the DMA controller which is set by user program is decremented. Initially the TC pin is low. When terminal count register become zero the TC signal become high. The TC is enabled by Mode set register. When the



timer recognizes the TC signal it resets the pulse count in the buffer. Before the TC become high the pulses from the free running timer is counted by a buffer. The buffer will count the number of the pulses until the terminal count register value is zero. When it is zero the TC will enable the Output enable pin of the buffer which allow to write the data from buffer into memory. When the encoder pulse width is large terminal count register will take more time to reach zero. So the buffer will store maximum count pulses from the free running timer. If the encoder pulse width is small in case of high speed the number of pulses stored in the buffer will be minimum. So the number of pulses in the buffer is counted which indicates the speed of the disk or the number of pulses arrived at DRQ.

V. Software Routines

Step1: mask the channel which is used to access the peripheral

Step2: Enable TC stop bit and Auto reload bit of mode set register.

Step3: After the TC pin enables the buffer unmask the channel.

Step4: Repeat from step1 to step 4 as per the user requirement to take the average values.

The code is developed in assembly level language using MASM software. The code can also be compile and execute in personal computer the debug level by giving internal DMA port addresses[6].

VI. Experimental setup

The 16 bit microprocessor is used to control the DMA controller. The microprocessor is operated at 5MHz clock frequency. The DMA controller is operated at 8MHz. The reference clock for the external free-running timer and the interval timer inside the microcontroller, f_{REF} is 2 MHz. The terminal count DMA method is verified using 20MHz Frequency generator, a tachometer is interfaced to generate the pulses for DRQ of DMA. Two buffers are used in between DMA and Timer to make delay. The hardware delay is created to enable buffer output data pins before enabling the timer. The number of auto reload mode is decided by user program. It can also be set using timer reset signal by connecting more logic circuit.

VII CONCLUSIONS

The TC DMA method is very easy to interface. The cost effect is less when compared to other methods. It need less hard ware for measurement of speed. The TC DMA method reduces the power consumption. It avoids the time constraints in accessing the capture registers. The TC DMA allows to measure large range of frequencies. The measurement error has a zero average value and almost fixed value over a wide frequency range. Further the execution time can be improved using ARM processor.

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