

DESIGN AND ANALYSIS OF ENHANCED DADDA MULTIPLIER USING 5:2 COMPRESSORS

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ABSTRACT:- Multiplier is one of the important circuits used in digital electronics field particularly in digital signal processing such as convolution, filtering and analysis of frequency. There are different kinds of algorithms used in multipliers to attain better performance such as Array, Booth, Sequential, Dadda and Wallace tree multiplier were the different types of multipliers created using CMOS logic. The Dadda multiplier is a most recent and advanced multiplier circuit which can be used to reduce partial product bit further it will reduce total number of iteration within certain limitations. The enhanced Dadda multiplier with 5:2 compressors further reduces partial product bit and no. of state transitions and the proposed method will minimize the usage of total number of logic gates used. Though Array, Wallace tree multiplier offers higher power consumption. Additionally, Dadda multipliers with 5:2 compressors minimize delay, power consumption and provide high robustness. The simulation was done by using Xilinx tool.

Keywords: Dadda Multiplier, 5:2 compressors, CMOS, state transitions, power consumption, delay, area.

I. INTRODUCTION

In recent years, design of portable consumer electronic products has turned as a challenging issue for hardware developers [1]. Mobile phones and smart cards are some of the models of consumer electronic products. Adders and multipliers are the most important elements used in low power consumption applications [2].

Multipliers are essential components of digital systems and hence their power dissipation and speed are the main concern. The power consumption is the most important parameter for portable applications [3]. Multiplication plays an essential role in computer arithmetic operations for both general purpose and digital signal processors [4].

Digital signal processors (DSPs) are employed to perform the universal functions such as video processing; filtering, image processing and Fast Fourier Transform (FFT). Such modules achieve sequences of multiplication and accumulation operations. Huge number of transistors with higher switching transitions is utilized to implement variety of multiplication processes [5]. Multiplier uses up to 30% of power and it also uses 46% of chip area in Radix-4 FFT processor. Multiplier is the most critical arithmetic component which needs larger area and computational time period [6]. Many reports have been acquired to achieve the design of energy efficient multiplier. Variety of tree and array based multipliers are widely used in low power consumption and high speed applications. Array based multipliers utilize lower power and it has moderately higher performance compared to Wallace tree multipliers. Supplementary hardware is essential to enhance the performance of tree-based multiplier [7].

II. RELATED WORKS

8×8 Bit pipelined parallel multiplier uses Dadda scheme and this type of multiplier has been executed in 3μm CMOS process with two layers of metal using cell replacement and routing program. The pipelining design employs a new type of carry look ahead adder in the closing stage of summation and this provides an important impact to high performance multiplier and this design was operated at a frequency of 50 MHz [8].

Two well-known fast multipliers were presented by Dadda and Wallace and these multipliers use full adders and half adders in reduction phase. The modified Wallace tree reduces 80% of half adders. The partial products are also minimized. Finally, path carry select adder was used in final carry propagation [9].

Fast column compression multiplication has been acquired using combination of two different designs. One is dividing the partial products into two portions for independent parallel column compression and acceleration is achieved using hybrid adder. The performance of the column compressed multiplier was examined by analysing area, delay and power. The results demonstrated that 64-bit regular Dadda multiplier is

41.1% slower than fast column compression multiplier and also the power-delay product is considerably lower than fixed Dadda multiplier [10].

Power management has developed as a critical anxiety due to its portable applications. Many procedures at different levels of design procedures were used to reduce power dissipation. High speed multiplication is a major problem in high performance computing systems. 8×8 hybrid tree multiplier is implemented by linking Wallace and Dadda methods and the results demonstrated 40 % of power reduction [11]. The modifications of Wallace/Dadda Multiplier use carry look ahead adders as a replacement of full adders to implement the reduction in bit product matrix. Each carry look ahead adder reduces the stages up to 9 partial products and it leads to a few reduction stages compared to conventional Wallace/Dadda Multiplier [12].

Swing Restored complementary Pass-transistor Logic (SR-CPL) was created using n-MOS transistor that is derived from Complementary Pass Logic (CPL) logic which can be applied to the arithmetic building block and it delivers high speed. DADDA multiplier was implemented using ripple carry and carry save adder and the simulations were carried out by TANNER EDA tool [13].

Our present research work states that a novel design to attain low power and high speed multiplication process with reduced hardware. This multiplier accepts parallel design to improve the speed of action. 5:2 compression techniques are added to the existing Dadda multiplier to reduce the switching transition and to save power consumption. In addition, 8 bit multiplier circuit with lesser number of transistors is also implemented.

III. DESIGN OF DADDA MULTIPLIER

In multiplication scheme, final process of summation takes place in slower manner to attain the partial products. In parallel multiplier, partial products are created using combination of AND gates. The main difficulties in the summation of partial products was that will take larger time to perform particular operation [14]. The usual working process of Dadda multiplication scheme was shown in Figure 1.

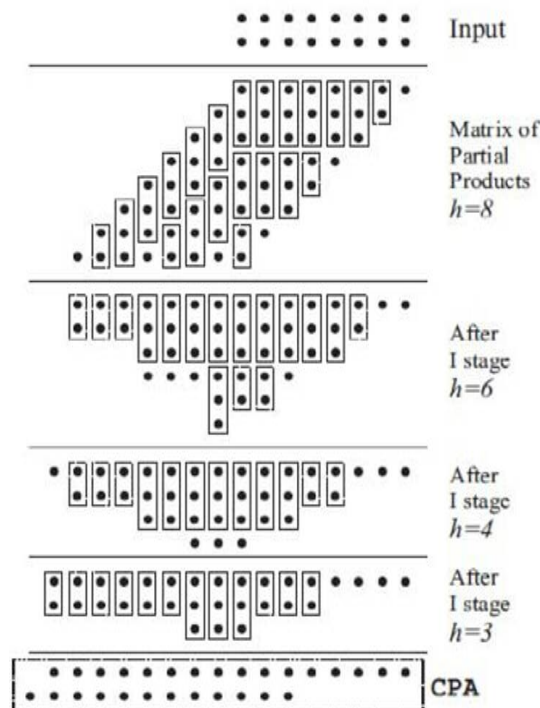


Figure 1 Dadda summation scheme – Regular process

Basically, Dadda scheme reduces number of adder phases that are needed to perform the summation of partial products and this can be achieved using full and half adders to minimize the number of rows in matrix at each summation phase. Dadda multipliers are refinement of parallel multipliers offered by Wallace. Dadda multiplier contains three phases. The partial product matrix is designed in the first phase by AND gate. In the second phase, the partial product matrix is minimized to the height of two. In third phase, Dadda multiplier substituted Wallace Pseudo adders through parallel counters. A Parallel counter is a circuit which has n inputs and creates m outputs which delivers a binary count of inputs [15].

The disadvantage of Dadda multiplier requires moderately wider fast Carry Propagate Adder (CPA) and it has less regular structure than Wallace. Figure 2 shows the schematic diagram of 8 bit Dadda multiplier. The reduction process of Dadda multiplier was developed using recursive algorithm:

- Step 1: Initialize n-bit multiplier and n-bit multiplicand
- Step 2: Formation of partial products using AND gate
- Step 3: Reduce the number of partial products by compressing the columns
- Step 4: Merge partial products with 5:2 compressor techniques
- Step 5: Finally, 2n-bit results are obtained

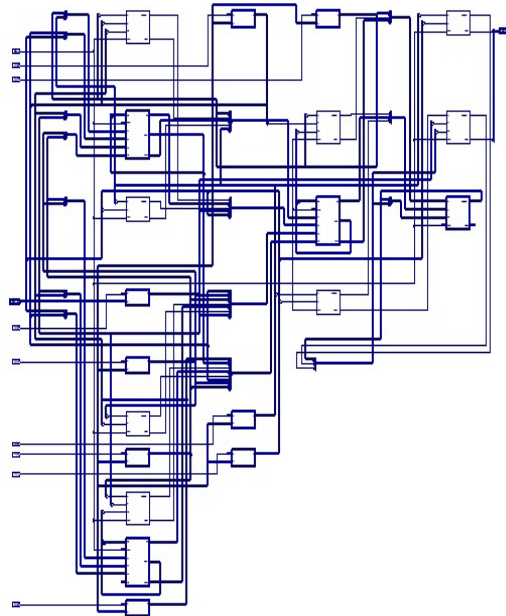


Figure 2 Schematic diagram of Dadda multiplier

Dadda multipliers reduce number of rows as much as possible on every layer; Due to this reason, Dadda multipliers produces less expensive reduction. In addition to this Dadda multiplier will reduce dynamic power dissipation and minimize total switching activity.

IV. PROPOSED DESIGN OF ENHANCED DADDA MULTIPLIER USING 5:2 COMPRESSOR

Dadda multipliers are refinement of parallel multipliers and offered by Wallace in 1964. In contrast to Wallace reduction Dadda multiplier achieve least reduction at every stage [4]. The maximum height of each phase is predicted from final stage which contains two rows of partial products. The height of the each phase will be in the order of 2, 3, 4, 6, 9, 13, 19, 28, 42, 63 etc. Reduction phase in modified Dadda multiplier with 5:2 compressor techniques was shown in figure 3.

Steps involved in DADDA multipliers with 5:2 compressor techniques:

- Multiply (AND operation) each bit by each bit of other arguments, obtaining N results
- Reduce the total number of partial products to 4 stages.
- Normal Dadda multiplier uses conventional adder (half adder, full adder and carry look ahead adder) but Dadda multiplier with compressor reduces the summation steps and state transition steps, delay and power consumption.

Partial product acquired after multiplication was obtained at the first stage. The data's are obtained with 3 wires and added using 5:2 compressors and then the carry of each stage was added with next two data in the same stage. Partial products reduced to two layers using compressors with same procedure. At the final stage, 5:2 compressor techniques are used to perform the product operation. Schematic diagram of Dadda multiplier with modified 5:2 compressors are shown in figure 4.

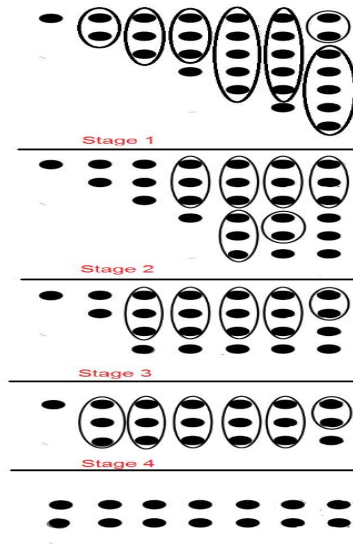


Figure 3 Reduction phase in modified Dadda multiplier with 5:2 compressor techniques

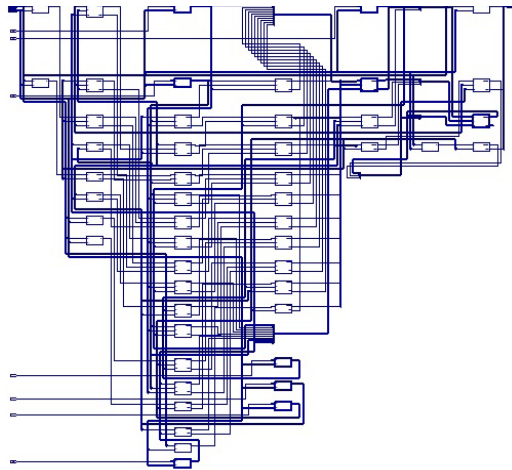


Figure 4 Schematic diagram of Dadda multiplier with modified 5:2 compressors

V. SIMULATION RESULTS AND DISCUSSION

The proposed multiplier was implemented using Xilinx tool and this tool was used to verify the 8 bit multiplication operation. Results of the proposed Dadda multiplier with compressors are compared with existing Dadda multipliers and Dadda multiplier with carry look ahead adder. All of them are designed at transistor level with a supply voltage of 0.9 V. The sizes of proposed multipliers are 8X8 bits.

5.1 Multiplication using Dadda multiplier with 5:2 compressors

In Dadda multiplication with 5:2 compressors uses 15 bits as multiplier and 15 bits as multiplicand, the output of the multiplication process produces 225 bits. Multiplication process using Dadda multiplier with 5:2 compressors was shown in figure 5.

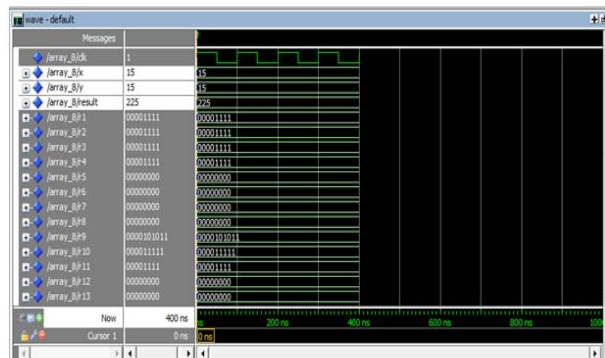


Figure 5 Multiplication process using Dadda multiplier with 5:2 compressors

Comparison between Table 1 (regular Dadda multiplier) and Table 2 (proposed Dadda multiplier) summarizes the enhanced performance of proposed multiplier. The proposed Dadda multiplier with 5:2 compressor techniques showed that the area of regular Dadda multiplier was considerably higher than the area of the proposed Dadda multiplier. The power consumption of proposed Dadda multiplier with compressor was 5.2% lower than the Dadda multiplier for 8-bit pattern. The power consumption of proposed Dadda multiplier will increase while increasing the word size.

The delay values obviously indicated that the proposed multiplier is always faster than the regular Dadda multiplier due to the reduced number of state transitions, also if there is an increase in word size, the delay will increase moderately. Regular Dadda multiplier and parameter estimation of Dadda multiplier with 5:2 compressor techniques was shown in Table 1 and Table 2.

TABLE 1. REGULAR DADDA MULTIPLIER

Multiplier N by N	Area (μm^2)	Delay (ns)	Power (μW)	Transistor count
8 by 8	8428	3.40	6.32	1536
16 by 16	29169	4.71	33.09	3148
32 by 32	105237	5.92	210.50	7518
64 by 64	397146	7.54	925.92	14125

TABLE 2. PARAMETER ESTIMATION OF DADDA MULTIPLIER WITH 5:2 COMPRESSOR TECHNIQUES

Multiplier N by N	Area (μm^2)	Delay (ns)	Power (mW)	Transistor count
8 by 8	7546	2.45	75	822
16 by 16	18654	3.85	60	1584

VI. CONCLUSION

In microprocessors, multiplication operation can be implemented using wide variety of methods. Minimization of power is one of most important operation in multipliers. We have accomplished faster multiplication by using the combination of two design techniques; partitioning of the partial products into two parts to perform multiplication operation and fast final addition using 5:2 compressor techniques. The result analysis showed that the power consumption, speed and area overheads are significant compared to existing Dadda multiplier. The proposed multiplier design technique can be executed with any kind of parallel multipliers to attain faster performance.

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