End to End delay analytical estimation of NoC with VBR traffic

Neila MOUSSA
EμE Lab, University of Monastir

Farah Nasri
EμE Lab, University of Monastir

Rached TOURKI
EμE Lab, University of Monastir

Abstract—
Network On Chip (NoC) integrate real time application that require strength performance guaranties, usually enforced by a tight upper bound on the maximum end-to-end delay. The complex and unpredictable nature of data traffic, initiate the use of modeling and analytical prediction. In this paper, a Network Calculus mathematical method is used for analyzing the worst delay for mesh NoC with variable bit rate(VBR) flow. The key idea of our proposed method involves presenting and proving a technical proposition to derive delay bound under the mentioned system model.

Keywords-component; ***Network on chip (NoC); Network Calculs(NC); Variable Bit Rate (VBR)***

I. INTRODUCTION

In NoC, cores are connected to each other through a network of routers and they communicate among themselves through packet-switched communication. So the congestion will take place in the Switch. That implies that current majority of work are focused on switch [1] [2].
The main challenge on the NoC is to conceive a switcher which accomplish the requirements needed on the communication and on the on chip-design. Switch has the responsibility to transmit the data through the NoC, which implies that the congestion will take place in Switch and can generate a high completion period. However current majority of work are focused on switch in the networks on chip [1] [2], considering it is the key element in architectures.
The complexity of the switch design mainly depends on the size of the buffer and the processing time of a flit. If the design lacks sufficient buffer space, the buffers may fill up too fast [3] [4] while over provisioning of buffers visibly is a waste of scarce area resources. Even as the buffer size it influences the total size of the switch and the reduced delay is crucial to make a success of the communication in real time.
From where the need to conjoint the characteristics of the networks, such as delay and congestion, and the characteristics of design on chip, such as buffer space and energy, is the ideal way to guarantee the NoC quality of service. So the (NoC) communication technique was being a research field which still requires much intervention. For NoC performance estimation tools can be classified in simulation models and analytical models. Most researches use directly the simulation [5] [6] [7] or hardware implementation [1] for NoC switch evaluation. However, due to growing Network-on-Chip complexity and communication parallelism and in the context of the increasing importance of a tight time-to-market, formal and analytical methods are finding their place in system-on-chip design flow.
In this paper, we present and prove the required proposition for calculating output arrival curve under switch of NoC topology with analytical approach using network calculus theory [8]. Arrived curve was assumed as VBR class of traffic in which the rate can vary significantly and containing bursts. In [8] the real-time VBR flows was characterized by (L, p, σ, ρ) parameters. L represents the maximum transfer size, p peak rate, σ the burst value, and ρ average rate. In [3] authors optimize the regulation parameters aiming for buffer optimization with the use of VBR traffic. They use for switch service the rate latency which is not optimal since it mentions the work completed during a cycle in one moment without taking into account the progressive character of this work
Author in [9] present a theorem for calculating per-flow output arrival curve in tandem networks of rate-latency nodes traversed by leaky-bucket shaped flows. This theorem investigates computing output traffic

characterization only for average behavior of flows while the proposed proposition in this paper considers both average and peak behavior, which results in a more correct analysis.
This paper is organized as follows: In section II we give a network calculus background. In section III the model of NoC and switch architecture as the theory concept using NC. Then we present in section IV the worst delay bound. Finally we conclude this work sited the future objectives

II. NETWORK CALCULUS

f(t) and g(t) be wide-sense increasing functions defined for real number t $\geqslant$ 0, and f (0) = g(0) = 0. then their convolution under min-plus algebra is defined as:

$$(f \otimes g)(t) = \inf_{0 \leq s \leq t} \{ f(t-s) + g(s) \} \quad \textbf{(1)}$$

and their de-convolution is defined as:

$$(f \oslash g)(t) = \sup_{s \geqslant 0} \{ f(t+s) - g(s) \} \quad \textbf{(2)}$$

B. Definition 2 (Arrival Curve and TSPEC)

TSPEC (traffic specification), the arrival curve is characterized by :

$$\alpha(t) = \min(L + pt, \sigma + \rho t) \quad \textbf{(3)}$$

In witch L is the maximum transfer size, p the peak rate ($p \geq \rho$), σ the burstness ($\sigma \geq L$) , and ρ the average rate.

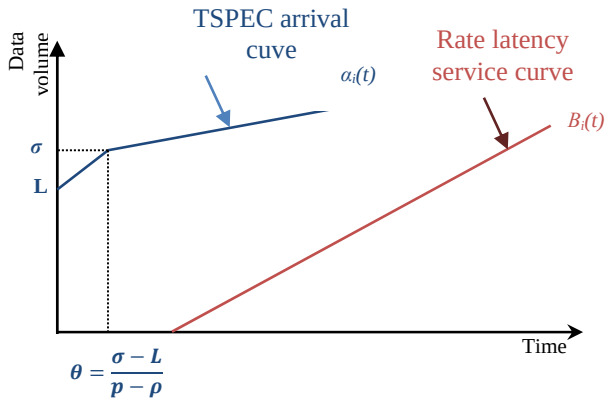


Fig1. The model of NoC switch architecture

C. Definition 3 (service curve)

A well-defined service curve is latency rate $\beta_{R,T}$

$$\beta_{R,T}(t) = R(t-T)^{+} \quad (4)$$

Where R is the service rate and T the maximum response delay.

D. Theorem 1 (Delay bound)

Assume a traffic flow constrained by arrival curve α(t), traverses a system that provides a service curve β (t). at any time t, the delay D(t) satisfies,

$$D(t)_{t \geq 0} \leq \inf_{\tau \geq 0} \{ \alpha(t) \leq \beta(t+\tau) \} \quad \textbf{(5)}$$

The delay bound define the maximum delay that would be experienced by a flit arriving at time t. Graphically the delay bound is the maximum horizontal deviation between α(t) and β (t).

E. Theorem 2 (Backlog bound)

Assume a traffic flow constrained by arrival curve α(t), traverses a system that provides a service curve β (t). The backlog B(t) for all t satisfies,

$$B(t) \leq \sup_{t \geq 0} \{ \alpha(t) - \beta(t) \} \quad \textbf{(6)}$$

The backlog bound is the amount of bits that are held inside the node. the required buffer size of a switcher is determined by the maximum backlog. Graphically, the backlog bound is the maximum vertical deviation between α(t) and β (t).

F. Theorem 3(Output bound)

Assume a traffic flow constrained by arrival curve α(t), that traverses a system that provides service curve β (t). The output flow is constrained by the following arrival curve,

$$\alpha^{*}(t) = sup_{s\geq 0}\{\alpha(t+s) - \beta(s)\} \quad \textbf{(7)}$$

G. Definition 7 (Concatenation)

Assume a traffic flow traversing tow systems which offers respectively a service curve β1(t) and β2(t). The concatenation of the tow systems offers the β(t) flows service, defined by,

$$B(T) = (B1 \otimes B2)(T) = INF_{0\leq S\leq T}\{B1(T-S)+B2(S)\} \quad \textbf{(8)}$$

III. NoC SWITCH MODEL

NoC architecture based of processing elements (PEs) and switcher. In this paper we will interest of WK architecture vied in figure 2.

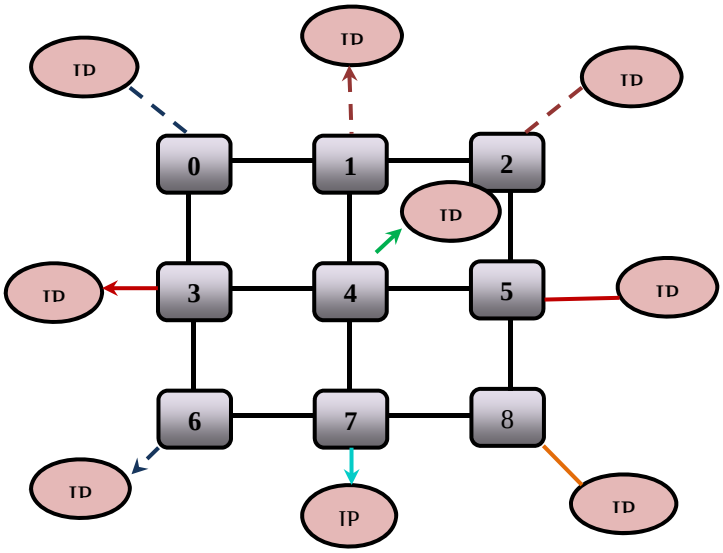


Fig. 2 Mesh network on chip architecture

.

The Switch model in figure 3 consist of an n ϵ N* input buffers, an arbitration routing unit. The policy considered is such as for (n ϵ N*) input ports, the multiplexer treats in success each port in a pre-established order; and this in a cyclic way.

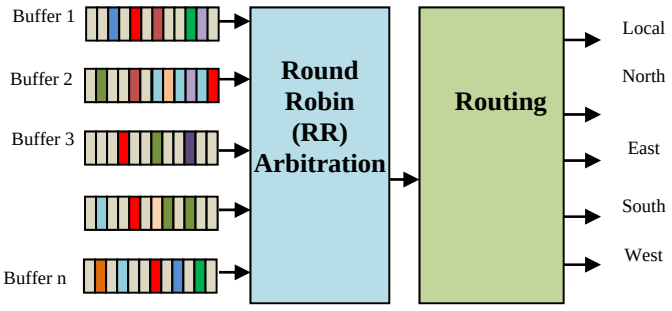


Fig3. The model of NoC switch architecture

IV. WK NoC SWITCHER SERVICE CURVE

The de-multiplexer achieves the flit to her destination output port. We notes β_F the file service curve β_M the multiplexer service curve, β_D the de-multiplexer service curve.

For the waiting in queue FIFO, the associated curve of service could be defined by the flowing expression .It shown the absence of treatment before a time τ equivalent to one horologe cycle.

$$\beta_F(t) = \begin{cases} \infty & \forall\, t \geq \tau \\ 0 & \forall\, t < \tau \end{cases} \quad \textbf{(9)}$$

The router is modeled as de-multiplexer and takes one τ delay to execute head (H) flit, and 2 τ for data (D) flit or end of packet (EOP) flit. The associated service curve is defined by:

$$\beta_D(t) = \begin{cases} \infty & \forall\, t \geq 2\tau \\ 0 & \forall\, t < 2\tau \end{cases} \quad \textbf{(10)}$$

The equation shows that the flit management in the de-multiplexing block is raised by 2 τ.

The multiplexer offering a service to a flow i is characterized by an average transmission rate $\rho_i \leq \frac{L\,F}{3\,\tau\,FN} \leq \frac{S}{\tau}$ where N is the number of input buffer and F the number of flit to transmit from one buffer in each cycle .The parameter 3τ integrates the flit management during three steps of a cell .

Then, it is possible to shape the service curve according to the considerations previously presented.

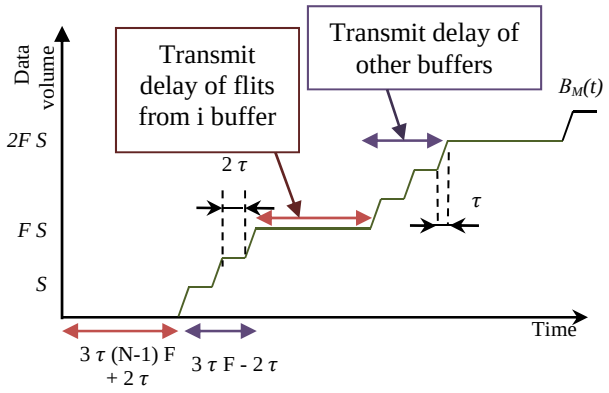


Fig.4 Round Robin multiplexer service curve

In the net we will utilize the notation illustrated in the table 1.

TABLE I. UTILISATION NOTATIONS

Notations	***Significations***
K_1	*Completely treated Flits number during the last Round Robin cycle.*
K_2	*Completely past Round Robin cycle number.*
S	*Flit size*
β_i	*Service curve offred for a buffer i by the R*

Using iteration methods, we will shown the round robin multiplexer service curve by the following expression

$$\beta_M(t) = \inf_{k_2 \in \mathbb{N}}\{k_2 FS + \inf_{k_1 \in \mathbb{N}}\{k_1 S + \frac{S}{\tau}(t - (k_2 NF + k_1)3\tau - 3\tau(N-1)F - 2\tau)^+\}\} \quad \textbf{(11)}$$

The service curves theorem composition implies that wired switcher service curve for buffer i is given by $\beta_F \otimes \beta 2_M \otimes \beta_D$, that is to say:

$\beta_i = \beta_F \otimes \beta_M \otimes \beta_D = \inf_{0 \leq s \leq t} \{\beta_F (t-s) + \beta_M (t) + \beta_D (t-s)\}$

Proposition 1 switch service curve

The service curves provided by a wired switch to a buffer i is given by:

$$\beta_i(t) = \inf_{k_2 \in \mathbb{N}}\{k_2 FS + \inf_{k_1 \in \mathbb{N}}\{k_1 S + \frac{S}{\tau}(t - (k_2 NF + k_1)3\tau - 3\tau(N-1)F + \tau)^+\}\} \quad \textbf{(12)}$$

V. WORST BOUND DELAY

We previously rappelled the theorem of delay that assume for a flow constrained by arrival curve α and traverses a system that offers a service curve β. The worst delay is constrained by $D(t)_{t\geq 0} \leq \inf_{\tau \geq 0} \{\alpha(t) \leq \beta (t+\tau\}$. Figure illustrated arrived and service curve.

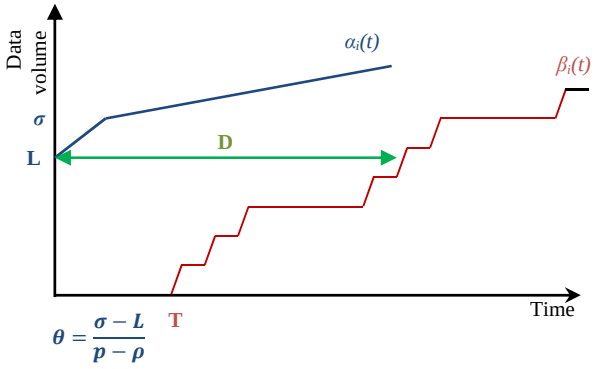
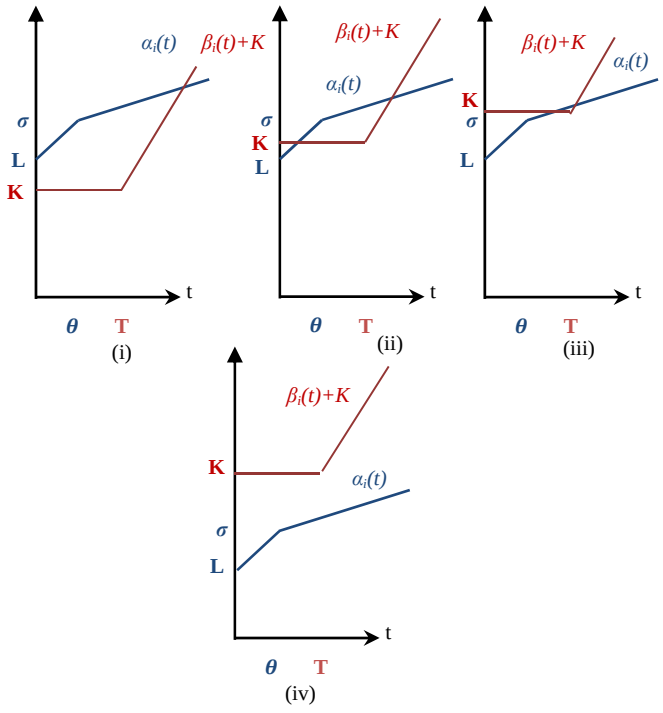
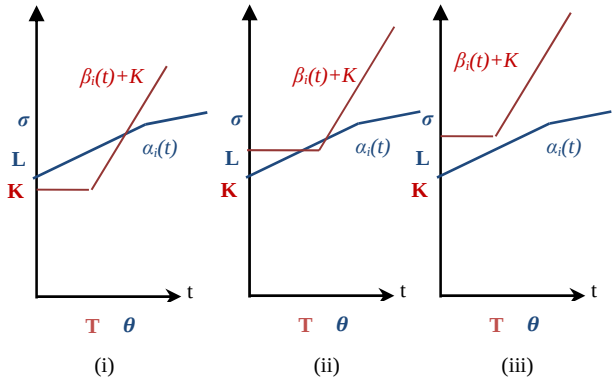


Fig.5 Curve of arrival and service, distances horizontal and vertical.

We consider the calculation of raising time of one flow constrained by α(t) crossing a system defines by the service curve K + β(T) such as:
$\alpha(t) = \min(L + pt, \sigma + \rho t)$ and $\beta_i(t) + K = K + R(t - T)^+$
We can then differentiate seven situations as shown in the Figure5; four cases when $\theta \leq T$ and three cases when $\theta > T$.



a- Cases when $\theta \leq T$ ((i) if $K \leq L$, (ii) if $L < K \leq \sigma$, (iii) if $\sigma < K \leq \sigma + \rho T$, and (iv) if $K > \sigma + \rho T$



b- Cases when $\theta > T$ ((i) if K≤L , (ii) if L < K ≤ σ , and (iv) if K> σ

Fig6. Curve arrival curve and service curve

Case $\theta \leq T$

(i) K≤L $d(t) \leq T + \frac{L-K}{R}$

(ii) L< K ≤ σ $d(t) \leq T + \frac{L-K}{R} < T$

(iii) σ < K ≤ σ +ρT $d(t) \leq T + \frac{\sigma-K}{R} < T$

(

(iv) K> σ +ρT, we can deduce directly that$d(t) \leq 0$.

In consequence taking into account the four results, delay solution is given by

$$d(t) = \begin{cases} T + \frac{L-K}{R} & if\ K \leq L \\ T + \frac{\sigma-K}{R} & if\ L < K \leq \sigma \\ T + \frac{\sigma-K}{R} < T & if\ \sigma < K \leq \sigma + \rho T \\ 0 & \end{cases} \quad \textbf{(14)}$$

Proposition 2 Switch delay bound

The crossing delay bound of flow i, constrained by an arrival curve $\alpha(t) = \min(L + pt, \sigma + \rho t)$ at the Switch crossing moment is raised by:

$$d(t) \leq 3\,\tau(N-1)F + 2\,\tau + \frac{L}{R} - \frac{FS}{R}\left\lfloor\frac{L}{SF}\right\rfloor - \frac{S}{R}\left(\left\lfloor\frac{L}{S}\right\rfloor + \left\lfloor\frac{L}{SF}\right\rfloor F\right) \textbf{(13)}$$

From calculation we can deduce the delay bound given by

$$d(t) = \begin{cases} T + \frac{L-K}{R} & if\ K \leq L \\ T + \frac{\sigma-K}{R} & if\ L < K \leq \sigma \\ T + \frac{\sigma-K}{R} < T & if\ \sigma < K \leq \sigma + \rho T \\ 0 & \end{cases} \quad \textbf{(14)}$$

The equation (14) can be reduced the max of the tow first case because in the third case d(t) <T and the last one the delay was null. And we now that L <σ so we will just consider the first case so

$$D(t) = T + \frac{L-K}{R}$$

We take here the development continuation of the equation (12) and we will integer in there the given results (the equation 13).

$$d(t) \leq sup_{k_1,k_2}\left\{T + \frac{L-K}{R}\right\}$$

$$\leq sup_{k_1,k_2}\left\{3\tau(N-1)F + 2\tau + \frac{L-(k_2\,FS + k_1 S}{R}\right\}$$

In other words, more k1, k2 will be large, more the worst time is important. Since $k_2\,FS + k_1 S \leq L$ and $k_2 \leq F$

$$k_2 = \left\lfloor \frac{L}{SF} \right\rfloor,\ k_1 = \left\lfloor \frac{L - k_2 FS}{S} \right\rfloor = \left\lfloor \frac{L}{S} \right\rfloor - k_2 F$$

Then we give the final delay expression:

$$d(t) \leq 3\,\tau(N-1)F + 2\,\tau + \frac{L}{R} - \frac{FS}{R}\left\lfloor \frac{L}{SF} \right\rfloor - \frac{S}{R}\left(\left\lfloor \frac{L}{S} \right\rfloor + \left\lfloor \frac{L}{SF} \right\rfloor F\right)$$

In this paper, we consider a simple application mapped on NoC and show how to estimate delay bound. Figure 7 shows the task graph.

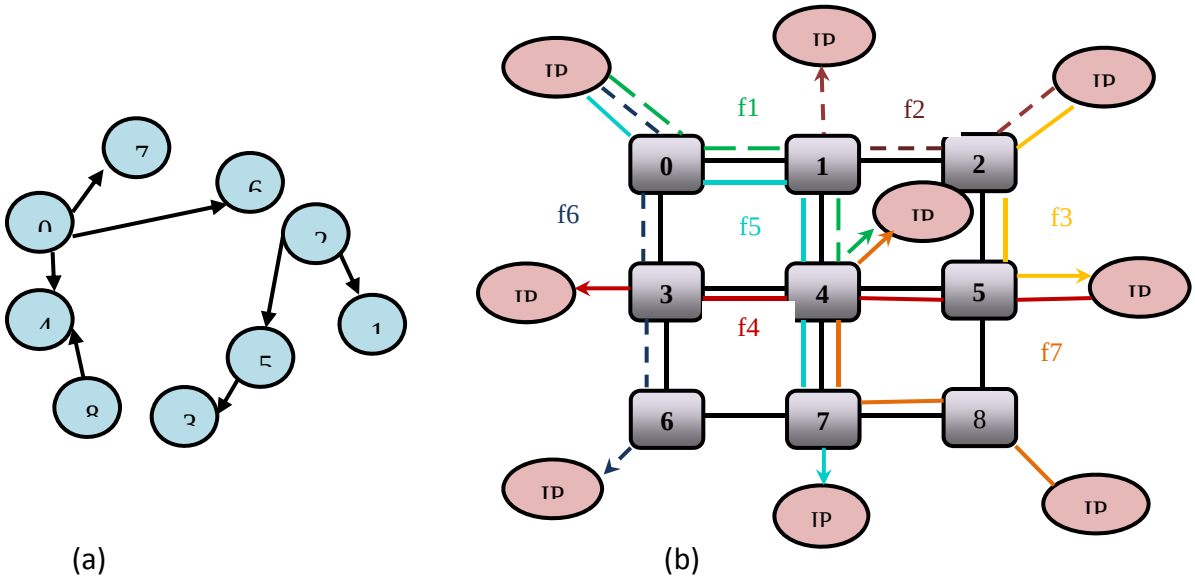


Fig 7. a) Task graph of an application mapped on an (b) NoC platform.

As illustrated in fig 2, the cores 0, 2, 5 and 8 are selected to be traffic sources. Cores 3,4,5,6 and 7 considered as sinks. We can see, in this traffic pattern, that core 0 and 2 are selected as a multi traffic source and core 4 is selected two times to be a traffic sink. The basic traffic supported by this architecture consists of messages divided in flits presenting all the same size. Links and routers are organized in a Mesh structure. Each VBR flow, have L, p, σ and ρ values, as well as route of the flow in the network. Data flows are represented by sequences of hops from a source core to a destination core. These data flows are computed using a deterministic routing protocol to direct flits between switches.

The basic traffic supported by this architecture consists of messages divided in flits presenting all the same size: 32 bits, 16bits, 64 bits. Links and routers are organized in a 3 × 3 mesh structure. Table III shows attributes of the traffic flows, including flow priority, source and destination of the flow, the values of sigma and rho, as well as route of the flow in the network. Data flows are represented by sequences of hops from a source core to a destination core. These data flows are computed using a deterministic routing protocol to direct flits between switches.

The exchanges considered are described in table (TabIV). The scale values of sigma and rho are adopted from the work presented in [SoC] and describing on chip communication with network calculus concepts.

TabIV

Flow	Weight	Priority	Source	Destination	σ (flits)	ρ (flit/cycle)	L (flits)	P (flit/cycle)	Data (flits)	Rho (flit/cycle)	Route
f1	w4	High	0	4	40	0.16			100	0.16	R0,R1,R4
f2	w3	medium	2	1	48	0.24			100	0.24	R2,R1
f3	w1	Low	2	5	40	0.24			700	0.24	R2,R5
f4	w4	High	5	3	40	0.16			100	0.16	R5,R4,R3
f5	w2	Normal	0	7	48	0.24			200	0.24	R0,R1,R4,R7
f6	w1	low	0	6	48	0.24			500	0.24	R0,R3,R6
f7	w3	medium	8	4	40	0.16			100	0.16	R4,R7,R8

As described in section 2, each switch classed buffer will be constrained by the weight W_n where N is the classe based weight. Classes based buffer weights value are 1, 2, 3, 4 related respectively to the w1, w2, w3r w4.

The output buffer of this data has will be obtained like seen in [11].

$$\alpha^*(t)= \sigma+D\rho$$

with D correspond to a total delay for the total input curves

Taking into account the topology and the policy of routing XY, it is possible to represent the traffics ways. The basic traffic supported by this architecture consists of messages divided in flits presenting all the same size: 32 bits, 16bits, 64 bits. Links and routers are organized in a 3 × 3 mesh structure. Table III shows attributes of the traffic flows, including flow priority, source and destination of the flow, the values of sigma and rho, as well as route of the flow in the network. Data flows are represented by sequences of hops from a source core to a destination core. These data flows are computed using a deterministic routing protocol to direct flits between switches.

As described in section 2, each switch classed buffer will be constrained by the weight W_n where N is the classe based weight. Classes based buffer weights value are 1, 2, 3, 4 related respectively to the w1, w2, w3r w4.

VI. CONCLUSIONS

On-chip networks expose a much larger design space to explore when compared with buses. The existence of a lot of design considerations at different layers leads to making design decisions difficult.

In this paper, we have proposed analytical study for the determination of delay with the use of VBR traffic, which can help to implement an efficient switch in NoC architecture. We have also given a summary of our analytical analysis of the proposed architecture with respect to baseline Mesh NoC architecture.

Our future research plans also to include a common analytical modeling and evaluation of mesh NoC architectural options.

REFERENCES

[1] P. Vellanki, N. Banerjee and K.S. Chatha, “Quality-of-Service and Error Control Techniques for Network-on-Chip Architectures”,ACM 2004

[2] C. A. Zeferino,F. G. M. E. Santo and A. A. Susin “ParIS: A Parameterizable Interconnect Switch for Networks-on-Chip” Proc. of IEEE Computer,35(1)2002.

[3] L-F. Leung and C-Y. Tsui “Optimal Link Scheduling on Improving Best-Effort and Guaranteed Services Performance in Network-on-Chip Systems” GLSVLSI’04, April 26–28, 2004, ACM.

[4] A. Kumar and R. Mahapatra "An Integrated Scheduling and Buffer Management Scheme for Input Queued Switches with Finite Buffer Space", Computer Communications 29 (2005) 42–51.

[5] E.Bolton, I.Cidon, R.Ginosar and A. Kolodny “QNoC: QoS architecture and design process for network on chip” Journal of system architecture ACM,50, 105 – 128, February 2004.

[6] B. Ahmad, A.T. Erdogan, S. Khawam “Architecture of a Dynamically Reconfigurable NoC for Adaptive Reconfigurable MPSoC” Conference on Adaptive Hardware and Systems (AHS'06),IEEE 2006.

[7] Terry Tao Ye, Luca Benini , Giovanni De Micheli, Packetization and routing analysis of on-chip multiprocessor networks. Journal of Systems Architecture 50 (2004) 81–104.

[8] J-Y. Le Boudec and P. Thiran T. J Network Calculus; A Theory of Deterministic Queuing Systems for the Internet”, LNCS 2050, 2001.

[9] L. Martorini, E. Mingozzi, and G. Stea, “Tight end-to-end perflow delay bounds in fifo multiplexing sink-tree networks”, Performance Evaluation, vol. 63, no. 9, pp. 956-987, 2006.