iImplementation of AMBA AHB protocol for high capacity memory management using VHDL

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Abstract- Microprocessor performance has improved rapidly these years. In contrast memory latencies and bandwidths have improved little. The result is that the memory access time is the bottleneck which limits the system performance. In case of larger system design which requires more number of I/O ports and more memory capacity the system designer may interface external I/O ports and memory with the system. In this paper we are using advanced microcontroller bus architecture with its advanced high performance bus. AMBA AHB provides parallel communications with multi master bus management, high clock frequency, high performance systems for data transfer operation from the memory interfaced with the master or slave peripheral devices. AMBA AHB supports on chip communications standard for designing high-performance embedded microcontrollers.

Keywords: AMBA, VHDL, ASB, APB, DMA, EDA

ROM, RAM, System-on chip,

1. Introduction- AMBA is an open specification that specifies a strategy on the management of the functional blocks that sort system on chip (SoC) architecture. It is a high-speed, high-bandwidth bus that supports multi master bus management to get the most out of system performance. AMBA specifications are able to maximize the use of system bus bandwidth during dead time. After defining a common backbone for SoC modules, it enhances a reusable design methodology. This system has emerged as the defect standard for IP library progress and SoC interconnection. The main goal of paper is to develop simulation for high capacity memory management to enhance the system performance and reduce the memory excess time. Thus AMBA AHB is suitable for the efficient connection of processors on chip memories and off chip external memories interface with low power peripheral macro cell functions.

2. AMBA AHB - The Advanced Microcontroller Bus Architecture (AMBA) specification defines an on chip communications standard for designing high-performance embedded microcontrollers.

Three distinct buses are defined within the AMBA specification:

• The Advanced High-performance Bus (AHB)

• The Advanced System Bus (ASB)

• The Advanced Peripheral Bus (APB).

A test methodology is included with the AMBA specification which provides an infrastructure for modular microcells test and diagnostic access.

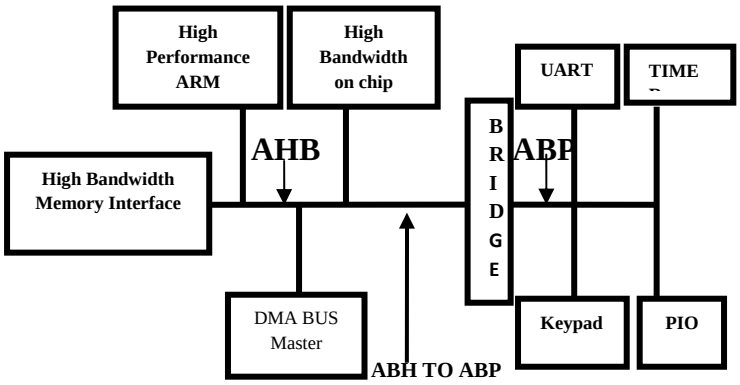

Fig 2 AMBA based microcontroller system

2.1 Advanced High-performance Bus (AHB)

The AMBA AHB is for high-performance, high clock frequency system modules. The AHB acts as the high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral macro cell functions. AHB is also specified to ensure easiness of use in an competent design flow using synthesis and automated test techniques.

2.2 Advanced System Bus (ASB)-The AMBA ASB is for high-performance system modules. AMBA ASB is an alternative system bus suitable for use where the high-performance features of AHB are not required. ASB also supports the efficient connection of processors, on-chip memories and off chip external memory interfaces with low-power peripheral macro cell functions.

3. Advanced Peripheral Bus (APB)-The AMBA APB is for low-power peripherals. AMBA APB is optimized for least power consumption and reduced interface complexity to support peripheral functions. APB can be used in conjunction with either version of the system bus.

3.1 Bus interconnection - The AMBA AHB bus protocol is considered to be used with a central multiplexor interconnection system. Using this method all bus masters drive out the address and control signals representing the transfer they wish to execute and the arbiter determines which master has its address and control signals routed to all of the slaves. A central decoder is also necessary to control the read data and response signal multiplexor, which selects the suitable signals from the slave that is implicated in the transfer.

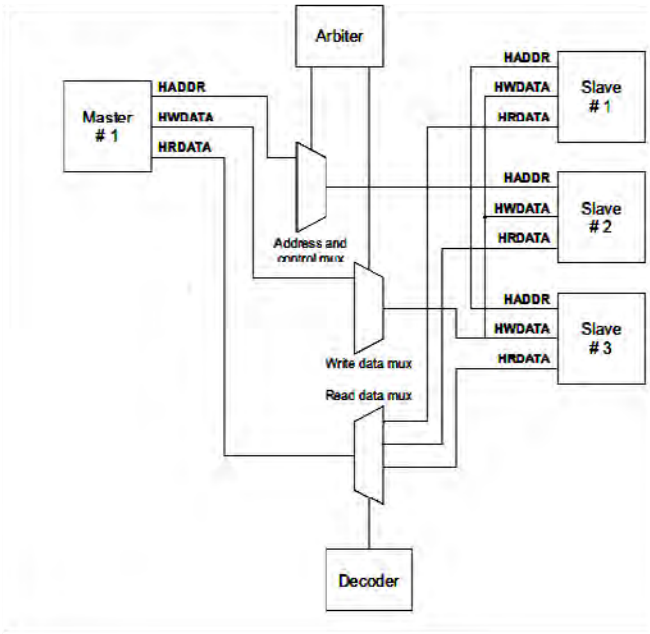

Fig 3.1 Multiplexor interconnection

AHB is a new generation of AMBA bus which is proposed to address the requirements of high-performance synthesizable designs. It is a high-performance system bus that supports multiple bus masters and provides high-bandwidth operation.

AMBA AHB implements the features required for high-performance, high clock frequency systems including:

- Burst transfers
- Split transactions
- Single-cycle bus master handover
- Single-clock edge operation
- Non-Tristate implementation• Wider data bus configurations (64/128 bits).

Bridging between this higher level of bus and the current ASB/APB can be done efficiently to ensure that any existing designs can be easily integrated. An AMBA AHB design may have one or more bus masters, typically a system would contain at least the processor and test interface. However, it would also be common for a Direct Memory Access (DMA) or Digital Signal Processor (DSP) to be included as bus masters.

3.2 AMBA AHB signal list -This section contains an overview of the AMBA AHB signals All signals are prefixed with the letter H, ensuring that the AHB signals is differentiated from other similarly named signals in a system design.

Name	Source	Description
HCLK Bus clock	Clock source	This clock times all bus transfers. All signal timings are related to the rising edge of HCLK.
HRESETn Reset	Reset controller	The bus reset signal is active LOW and is used to reset.
HADDR [31:0]	Master	The 32-bit system addresses bus.
HTRANS [1:0]	Master	Indicates the type of the current transfer, which can be..
HWRITE Transfer direction	Master	When HIGH this signal indicates a write transfer and when LOW a read transfer.
HSIZE [2:0] Transfer size	Master	Indicates the size of the transfer, which is typically byte (8-bit), halfword (16-bit) or word (32-bit).
HBURST [2:0]	Master	Indicates if the transfer forms part of a burst.
HPROT [3:0]	Master	The protection control signals provide additional information
HWDATA [31:0] Write data	Master	The write data bus is used to transfer data from the bus master to the bus slaves during write operations.
HSELx Slave select	Decoder	Each AHB slave has its own slave select signal and this signal indicates that the current
HRDATA	Slave	The read data bus is used to transfer data from bus slaves to the bus master during read operations.
HREADY Transfer done	Slave	When HIGH the HREADY signal indicates that a transfer has finished on the bus.
HRESP [1:8]	Slave	The transfer response provides additional information on the status of a transfer.

3.3 AHB arbiter -The role of the arbiter in an AMBA system is to control which master has access to the bus. Every bus master has a REQUEST/GRANT interface to the arbiter and the arbiter uses a prioritization scheme to decide which b us master is currently the highest priority master requesting the bus. Each master also generates a HLOCKx signal which is used to indicate that the master requires exclusive access to the bus. The detail of the priority scheme is not specified and is defined for each application. It is acceptable for the arbiter to use other signals, either AMBA or non AMBA, to influence the priority scheme that is in use.

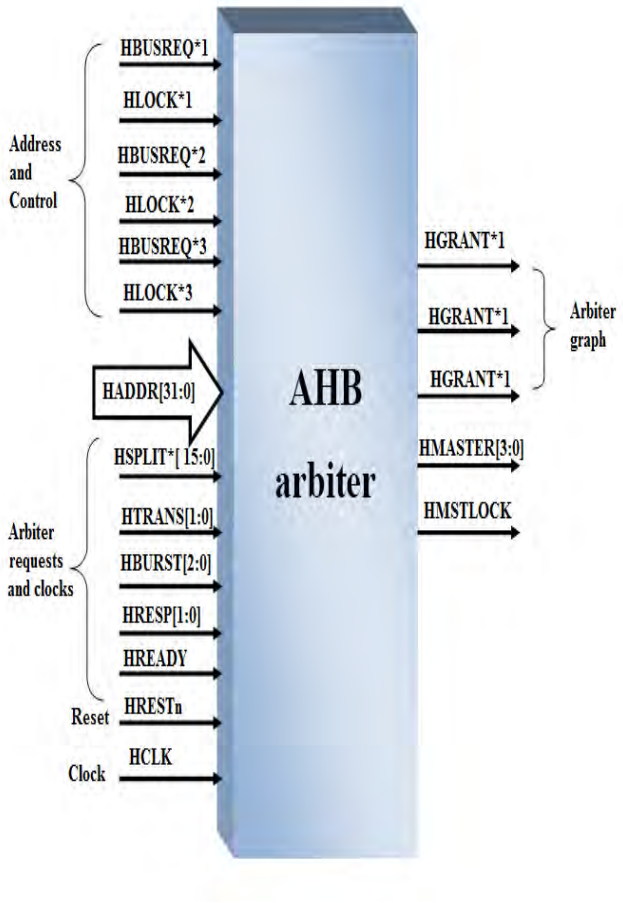

Fig 3.1 AHB arbiter interface diagram

3.4 Implementation of AMBA AHB with Memory compliant -The AMBA AHB protocol is design and simulated with VHDL to verify and validate the AMBA specification. The master is connected with the memory device. The data from the memory is written by the master and arbiter permits the master to send its data for read operations by the slave with the help of decoder to select that which slave will read the data send by the master.

4 RESULTS ON MODELSIM USING XILINX ISE AND VHDL - The overall coding part can be writing on VHDL and simulate on ModelSim

4.1 Simulation Result of Reset -This simulation result contain hclk signal to give the clock all input and output signals. Then the signal hreset =1 is high with the hclk=1 to initialize all the signal. After initialization the signal hreset remains low for the further operation.

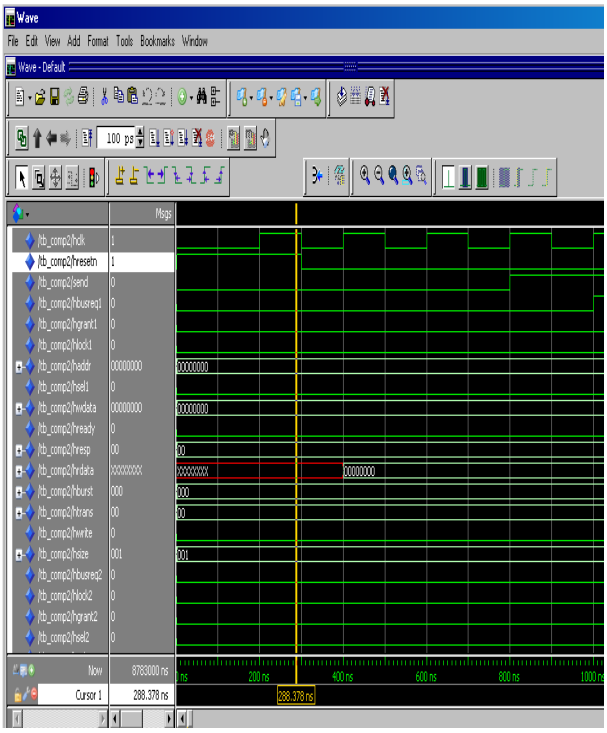

Fig.5.1 Simulation Result for initialize all the signals when hreset = 1

4.2 Simulation Result of Bus Request-This simulation result contain signal hreset=0 and the signal send=1 is send to the arbiter to initialize the data transfer. With send=1, hbusreq1=1 is also send to the arbiter which indicates that the bus master1 requires the bus for data transfer.

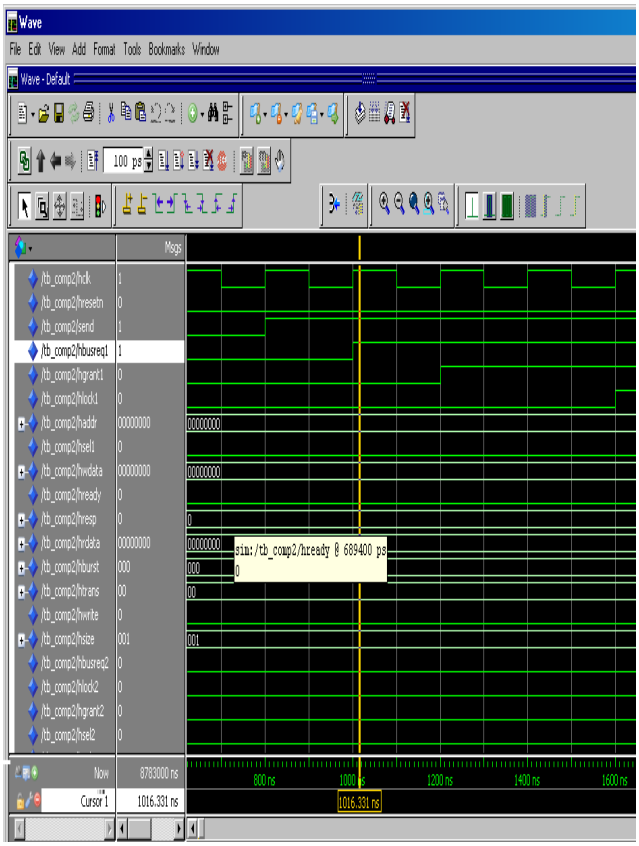

Fig.5.2 Simulation Result for the bus request when signal send =1, and hbusreq =1

4.3 Simulation Result of Arbiter -After sending the bus request to the arbiter, arbiter sends the signal hgrant1=1 to the master1, which shows that the bus master1 is currently at the highest priority. Ownership of the adderss control signal changes at the end of the transfer when hready is high but in this result hready=0.

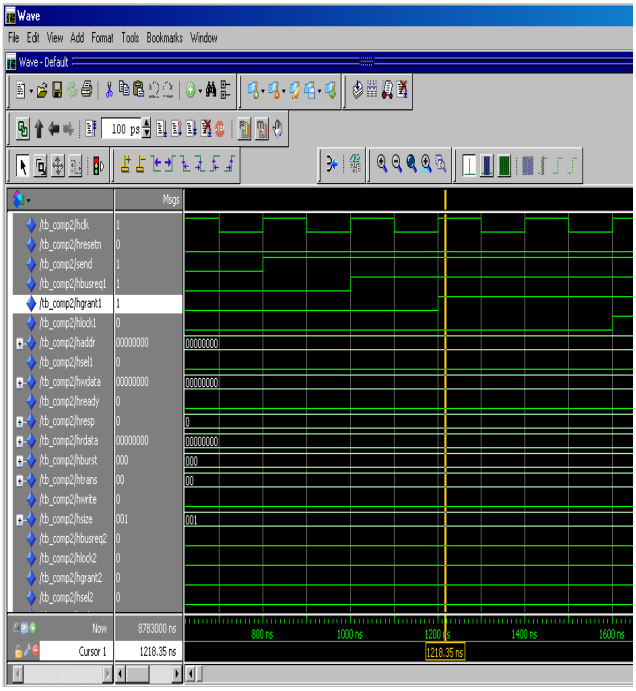

Fig.5.3 Simulation Result for signal hgrant=1 from the arbiter to the master1

5. CONCLUSION - In this thesis we observe that the data transfer operation from one memory to another memory is fast as compared to serial communication by proposing the parallel communication in AMBA AHB. It also provides the opportunity to use master and slave up to 16 nos. and the data of every master is read and write simultaneously. In this implementation delay period is 4.33 ns and the clock period is 8.66 ns and frequency increases up to 115.401MHz..Here AMBA AHB supports the data transfer by reducing the time and increases the frequency of the bus to increase the system performance. The use of high capacity memory management with the AMBA AHB in this thesis successfully attempted to find the software solution for the problem of memory compliant in the microcontroller. The proposed implementation is capable of running in any PC with Xilinx and Modelsim EDA tools and FPGA board. This implementation able to sustain the external memory bandwidth, on which the CPU, on-chip memory and other Direct memory access devices reside. This implementation supports external memory up to 2GB.

REFERENCES –

[1] "AMBA specification (Rev2.0)", ARM Inc.
[2] Hu Yueli,Yang Ben "Building an AMBA AHB compliant Memory Controller" in 2011.
[3] Ashutoshku.Singh, Anurag Shrivastava, G.S.Tomar" Design and Implementation of High Performance AHB Reconfigurable Arbiter for on-chip Bus Architecture "in 2011.
[4] Wei Chipin,Li Zhaolin,Zheng Qingwei,Ye Jianfei, Li Shenglong"Design of Configurable Multichannel Interrupt Controller "in 2010.
[5] Yi Zhiqiang, Li Yun"On Chip Bus Design for HDTV SOC Decoder" in 2010.
[6] Ramesh Bhakthatchalu, Deepthy G R, Shanooja S. "Implementation of Reconfigurable Open Core Protocol Complaint Memory System using VHDL" in 2010.
[7] Zhichao Zhang, Wuchen Wu "UART integration in OR1200 based SOC design" in 2010.
[8] Purvi D. Mulani "SOC Level Verification Using System Verilog" in 2009.
[9] Guoling Ma,Hu He "Design and Implementation of an Advance DMA Controller on AMBA-Based SOC "in 2009