A Mixed-Mode Signal Processing Architecture for Radix-2 DHT

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***Abstract*—This paper proposes a mixed-mode signal processing architecture for radix-2 DHT. In the known algorithms, the stage structures perform all the additions and multiplications. The proposed algorithm introduces multiplying structures which perform all the multiplications with the cosine coefficients and their related additions. This leads to i) simplification of the stage structures which now perform only the additions, and ii) a reduction in the number of multiplications without affecting the number of additions. A mixed-mode signal processing architecture to implement the algorithm utilizing an *N*-bit ring counter, sample-and-hold array and analog block structure is proposed. The validity of this design has been tested by simulating it with the help of Orcad PSpice.**

Keywords- Decimation-in-time; decimation-in-frequency; discrete Hartley transform; mixed-mode architecture; radix-2.

I. INTRODUCTION

The discrete Hartley transform (DHT) has been established as a potential tool for signal processing. An N-point one dimensional DHT X_H of a sequence $x(n)$ is defined as

$$X_H(k) = \frac{1}{N}\sum_{n=0}^{N-1} x(n)\,\mathrm{cas}\left(\frac{2\pi kn}{N}\right) \qquad k = 0, 1, \ldots, N\text{-}1, \qquad (1)$$

where cas (.) = cos (.) + sin (.).

The fast Hartley transform (FHT) algorithm introduced by Bracewell [1] performs the DHT in a time proportional to $N\log_2 N$ using decimation-in-time (DIT). Meckelburg and Lipka presented the decimation-in-frequency (DIF) FHT algorithm [2] claiming it to be faster than the one in [1]. Sorenson et al. [3] further analyzed the FHT having the same decomposition as [1], using the index mapping approach, implemented the algorithms for both DIT and DIF, and verified their operational complexities to be the same. Prado [4] presented an in-place version of the FHT in [1] along with its operational complexity. The signal flow diagram originally proposed in [1] has been restructured for clarity, and by applying the transposition theorem a DIF algorithm having the same operational complexity has been obtained by Kwong and Shiu [5]. The above approaches required computation of the cosine coefficients (CCs) and sine coefficients (SCs) which are stage-dependent. Hou [6] concluded that the FHT algorithm, in essence, is a generalization of the Cooley-Tukey fast Fourier transform (FFT) algorithm to compute the discrete Fourier transforms (DFT), but it requires only real arithmetic computations as compared to complex arithmetic operations in any standard FFT. Hao [7] examined both the pre- and post-permutation algorithms in [1] and [2] and suggested improvements to make them faster by use of fast rotation to reduce the multiplications and by incorporating in-place or distributed permutation. Malvar [8] presented a new factorization of the DHT which involves the discrete cosine transform (DCT). His algorithms minimize the multiplications at the expense of an increased number of additions. Rathore [9] reported, for both the DIT in [1] and the DIF in [2], that the operational complexity involved is the same. He further utilized the matrix approach, derived some properties of the DHT [10], obtained the relations for computational complexity and presented DHT-based DFT and DFT-based DHT algorithms.

Various architectures have been reported in the literature to compute the DHT. Chakrabarti and Jaja [11] have proposed a modular bit-level systolic architecture. Dhar and Banerjee [12] have employed a set of linear arrays of Givens rotors. Chang and Lee [13] have derived two models of linear systolic arrays and have suggested the use of cordic algorithms to make the systolic arrays more efficient in computation. Hsiao et al. [14] have modified the above cordic processor and obtained a higher throughput and cost effective architecture. Kar and Rao [15] proposed a unified systolic architecture for sliding window computation of discrete transforms. Nayak and Meher [16] have implemented a bit-level systolic architecture for discrete orthogonal transforms using a serial–parallel vector–matrix multiplication scheme based on the Baugh–Wooley algorithm. Guo [17, 18] presented two architectures; one using parallel adders and the other using a distributed arithmetic based array that utilizes identical ROM modules and eliminates the accumulation loop in the processing elements. Amira and Bouridane [19, 20] have developed architectures to implement the DHT on field programmable gate arrays. Meher et al. [21] have presented a design framework for scalable and modular memory based implementation of the DHT in systolic hardware. These architectures compute the DHT using digital VLSI techniques. However, there are architectures which compute the DHT based on analog blocks. Culhane et al. [22] presented an analog circuit which utilizes a linear programming neural net to compute the DHT. Raut et al. [23] presented basic switched capacitor building blocks in systolic array architecture to implement the DFT. A two dimensional DCT structure proposed by Kawahito et al. [24] has been designed with fully differential switched-capacitor circuits. Digitally controlled analog circuits have been proposed by Chen et al. [25] which utilize the principle of charge scaling for computing the DCT and DFT. Mal and Dhar [26] proposed an analog sampled data architecture for the DHT.

The growing computational demand for complex information processing has motivated significant research in the design of power efficient signal processing systems. One method for achieving low-power designs is to move processing on system inputs from the digital processor to analog hardware. However, for analog systems to be desirable to digital signal processing engineers, they need to provide a significant advantage in terms of size and power. They should be relatively easy to use and integrate into a larger digital system. Reconfigurable analog arrays, dubbed field-programmable analog arrays (FPAAs), can speed the transition of systems from digital to analog by providing the ability to rapidly implement advanced, low-power signal processing systems [27]. The drive towards analog integrated circuits has demanded the development of high performance analog circuits that are reconfigurable and suitable for CAD methodologies. If analog circuits are mixed with digital control, to meet the application requirements an analog-digital mixed system is obtained. In this mixed mode, sampled analog processing comes into picture. In analog signal processing level and time are continuous. In digital signal processing both level and time are discrete. In discrete-time signal processing (sampled analog processing) the level remains continuous but time is discrete. It is better for high frequency applications where time available for data conversion or for computations is limited. DSP algorithms can be used directly off-the-shelf with little or no modification. Analog circuits based on the current feedback operational amplifier (CFA) technique are suitable for high frequency applications [28]-[30].

In this paper we present the design of a simple, versatile, generalized and easy to implement basic analog circuit based on operational amplifiers. It can be easily reconfigured as a stage structure analog block or multiplying structure analog block. A mixed-mode signal processing architecture for the DHT utilizing these blocks along with a ring counter for digital control and a sample-and-hold array for converting the input into sampled analog data has been proposed.

II. THE PROPOSED ALGORITHM

The operation of the proposed radix-2 decimation-in-time algorithm is obtained as a sequence of matrix operations on the data. It has the same permutation matrix, P_r, as in [1]-[5]. It modifies the existing stage structure matrices (SSMs), L_S and introduces multiplying structure matrices (MSMs), L_{SM}, to simplify the computation. SSM performs only additions, and MSM performs the multiplications with the cosine coefficients (CCs) and their related additions and are introduced for the stages $2 < S < P$. The matrix formulation has been verified to obtain the DHT as $X_H = N^{-1} L_P L_{PM} L_{(P-1)} L_{(P-1)M} \cdots L_3 L_{3M} L_2 L_1 P_r x(n)$. A succession of P stage operations leads stage by stage to the outputs, $x_1(n)$ through $x_P(n)$.

A. Generalized Structure

Fig. 1 depicts a signal flow diagram (SFD) showing the generalized structure that consists of both the multiplying structure (MS) and the stage structure (SS). The introduction of L_{SM} in the expression of the DHT reflects in the form of a multiplying structure (MS) in the SFD which performs all the multiplications with the CCs and their related additions. The SFD for the SS is simple, follows a regular pattern and performs only additions. The structures are then utilized as per the algorithm to obtain the overall SFD. For each MS, there are multipliers for different elements as shown in Fig. 1.

Elements from 0 to $m/2$ have no multipliers. Each element $(m/2) + i$ has no multiplier for $i = m/4$, a multiplier 0.707 for $i = m/8$, and multipliers α_i, β_i for $i = 1$ to $(m/8) - 1$ and $(m/8) + 1$ to $(m/4) - 1$. Each element $m - i$ has a multiplier 0.707 for $i = m/8$, and multipliers $-\alpha_i$ and β_i for $i = 1$ to $(m/8) - 1$ and $(m/8) + 1$ to $(m/4) - 1$, where $\alpha_i = \cos\frac{2\pi i}{m}$ and $\beta_i = \cos\frac{2\pi}{m}\left(\frac{m}{4} - i\right)$ are the CCs other than 0.707. For each stage S from 3 to P, MSs are introduced, and the maximum number of CCs are required in the MS corresponding to the last stage $S = P$. The number of CCs in the MSs for the other stages is lesser and their values belong to the set of CCs for the last stage. Hence, for all the MSs, only $(N/4) - 1$ stage independent CCs are to be computed.

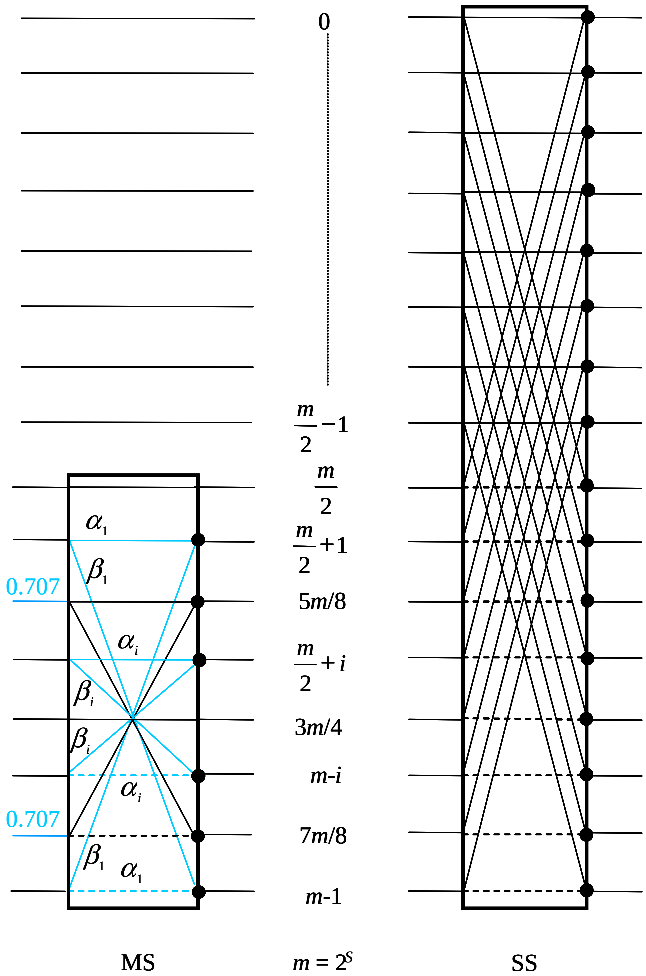


Figure 1. SFD for the generalized structure, $N = 2^P$

B. Operational Complexity

The known radix-2 algorithms [1]-[5], implement the FHT with operation counts of N_A additions and N_M multiplications given by

$$N_A = \frac{(3N\log_2 N - 3N + 4)}{2}, \qquad (2)$$

$$N_M = N\log_2 N - 3N + 4. \qquad (3)$$

The additions are performed by both the MS and SS. Number of MSs required per stage $= \frac{N}{m}$, where $m = 2^S$. Each MS requires $(m/2) - 2$ additions. Additions per stage $= \left(\frac{m}{2} - 2\right)\frac{N}{m} = \frac{N}{2} - \frac{2N}{m}$. The number of additions for all the MSs are $\sum_{S=3}^{P}\left(\frac{N}{2}-\frac{2N}{2^{S}}\right)$. Each SS requires N additions, for $N = 2^{P}$, the number of stages are P, hence, total number of additions for all the SSs = NP. For the entire SFD including all the MSs and SSs

$$N_A = \sum_{S=3}^{P}\left(\frac{N}{2}-\frac{N}{2^{S-1}}\right)+NP = \frac{(3N\log_2 N - 3N + 4)}{2}. \quad (4)$$

It is clear from (2) and (4) that N_A remains the same.

The multiplications are performed within the MSs. Each MS requires $m - 6$ multiplications. Multiplications per stage $= (m-6)\frac{N}{m} = N - \frac{6N}{m}$. The number of multiplications for all the MSs are

$$N_M = \sum_{S=3}^{P}\left(N - \frac{3N}{2^{S-1}}\right) = N\log_2 N - 3.5N + 6. \quad (5)$$

From (3) and (5) it is seen that N_M is lesser for $N \geq 8$ in the proposed algorithms as compared to the existing algorithms in [1] – [5]. It is evident that the number of non-trivial arithmetic operations is reduced by 2 multiplications (M) for each MS introduced. The reduction of $2M$ at the first stage is due to one MS corresponding to stage 1 and a reduction of $4M$ at the second stage is due to two MSs corresponding to stage 2. As the values of P and N increase, the MSs for the corresponding stages also increase, leading to a further reduction in the M. The total number of M reduces by $\frac{N-4}{2}$ for $N \geq 8$. The comparison of the operational complexities of the existing radix-2 algorithms with the proposed algorithm for various transform lengths is shown in Table I.

TABLE I. COMPARISON OF OPERATIONAL COMPLEXITIES

Length	**Radix-2 FHT algorithms [1]-[5]**			**Proposed Radix-2 Algorithm**		
N	***N_M***	***N_A***	***Total***	***N_M***	***N_A***	***Total***
8	4	26	30	2	26	28
16	20	74	94	14	74	88
32	68	194	262	54	194	248
64	196	482	678	166	482	648
128	516	1154	1670	454	1154	1608
256	1284	2690	3974	1158	2690	3848
512	3076	6146	9222	2822	6146	8968
1024	7172	13826	20998	6662	13826	20488
2048	16388	30722	47110	15366	30722	46088
4096	36868	67586	104454	34822	67586	102408

III. DESIGN OF ANALOG BLOCK STRUCTURE

Consider the circuit shown in Fig. 2.

The outputs are

$$V_1 = \left(\frac{R_1+R_2}{R_3+R_4}\right)\left[\frac{R_3}{R_1}V_A + \frac{R_4}{R_1}V_B\right], \quad (6)$$

$$V_2 = \frac{R_6}{R_5}\left(\frac{1+\frac{R_5}{R_6}}{1+\frac{R_7}{R_8}}\right)V_A - \frac{R_6}{R_5}V_B. \quad (7)$$

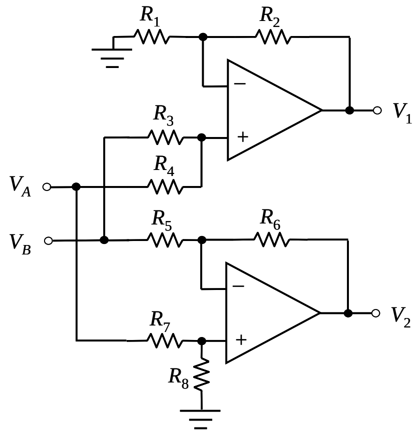


Figure 2. Basic analog circuit

Thus, the circuit acts as a weighted summer and subtractor.

Case (i): Choosing

$$R_1 = R_2 = R_3 = R_4 \text{ and } \frac{R_6}{R_5} = \frac{R_7}{R_8} = 1$$

$$V_1 = V_A + V_B, \tag{8}$$

$$V_2 = V_A - V_B. \tag{9}$$

Thus it may be utilized as a stage structure analog block (SAB).

Case (ii): Choosing

$$R_1 + R_2 = R_3 + R_4 \quad \frac{R_3}{R_1} = \frac{R_6}{R_5} = \alpha_i \quad \frac{R_4}{R_1} = \beta_i \text{ and } \frac{R_7}{R_8} = \left(\frac{\alpha_i + 1}{\beta_i}\right) - 1$$

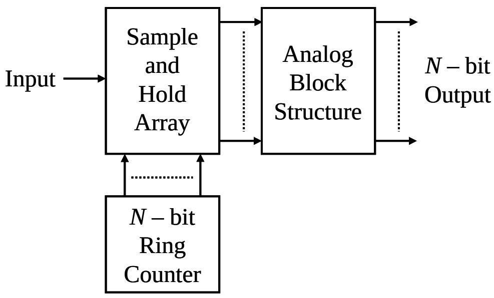
$$V_1 = \alpha_i V_A + \beta_i V_B, \tag{10}$$

$$V_2 = \beta_i V_A - \alpha_i V_B. \tag{11}$$

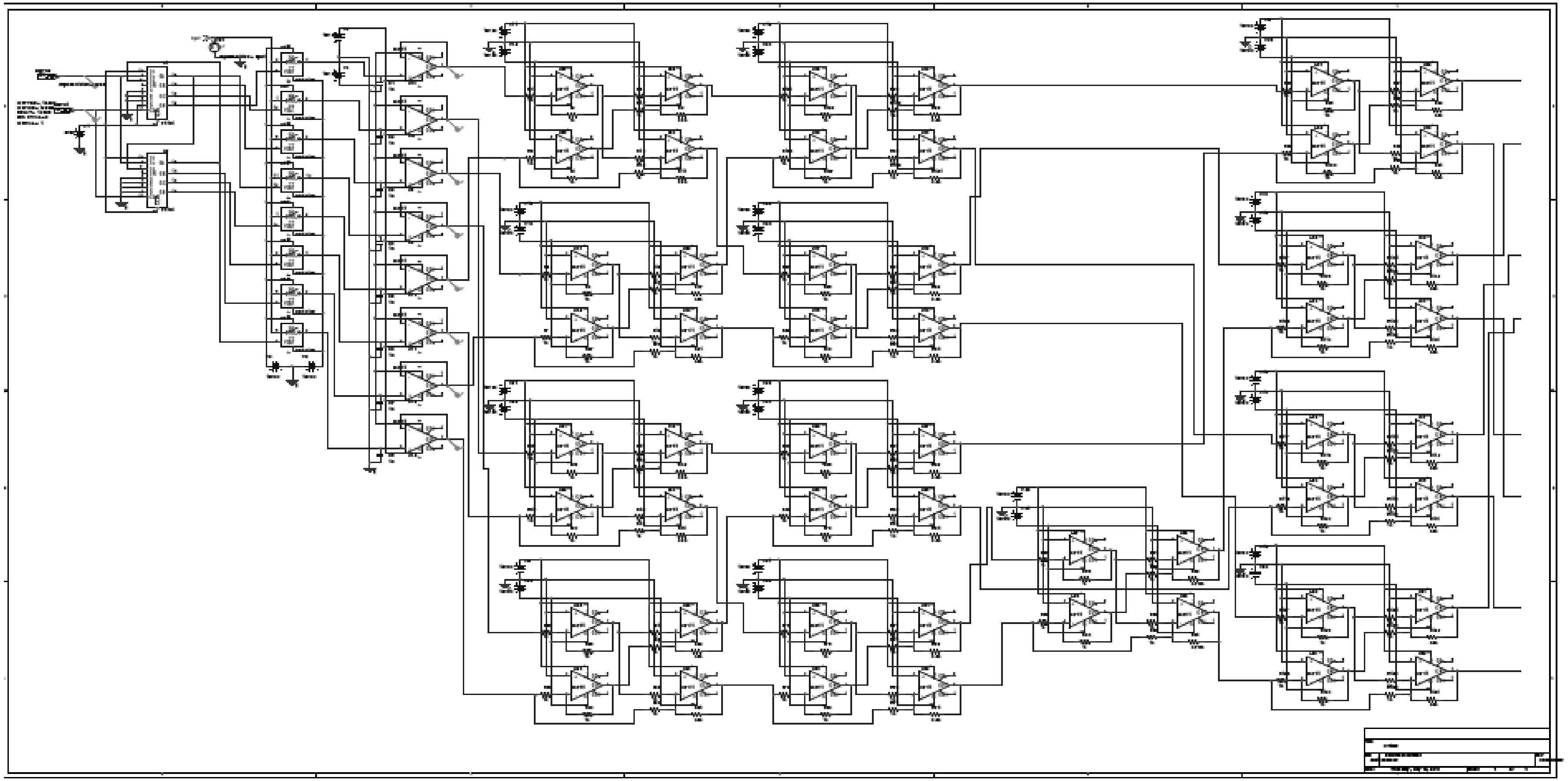
Thus it may be utilized as a multiplying structure analog block (MAB).

IV. THE PROPOSED ARCHITECTURE

The proposed mixed-mode signal processing architecture block diagram and corresponding circuit diagram for obtaining the DHT for $N = 8$ is shown in Fig. 3 (a) and (b) respectively. The latter is utilized for simulation in Orcad PSpice.



(a)



(b)

Figure 3. Mixed-Mode signal processing architecture for DHT (a) Circuit diagram for $N = 8$ (b) Block diagram

A. Ring counter

A shift register is an *N*-bit register with a provision for shifting its stored data by one bit position at each clock tick. The 74194 is an MSI 4-bit bidirectional parallel in parallel out shift register. Two such ICs are connected in cascade to form an 8 bit ring counter. The rightmost bit of the ring counter is pulled high and all the other seven bit are pulled low. This is utilized initially to load the counter with the pattern '0000-0001'. The S0 pins of the ICs are utilized to first load the pattern and then maintain the shift registers in the shift-left mode. At each clock tick the bit moves to the left and the patterns generated are 0000-0010, 0000-0100, and so on till finally the pattern is 1000-0000. On the next clock tick the pattern changes back to 0000-0001 due to the feedback and subsequently the sequence repeats. The ring counter does not count in an ascending or descending binary sequence, but is useful in control applications. The waveforms obtained at the output of the ring counter after simulation is as shown in Figure 4.

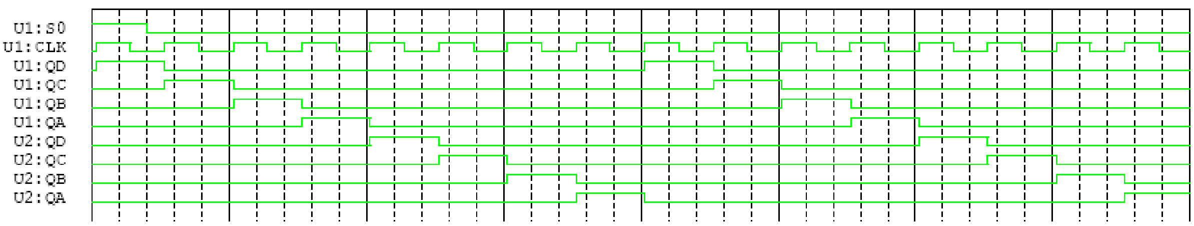


Figure 4. Waveforms obtained at the output of the ring counter

B. Sample and Hold

The basic sample and hold (SAH) circuit consists of a switch, hold capacitor and buffer amplifier. It has two basic and distinct operational states. In one state, the input signal is sampled and simultaneously transmitted to the output (sample). In the second, the last value of input sampled is held (hold) until the input is sampled once again. The ring counter digitally controls the SAH array. It asserts its output only one bit at a time from the first to the last and continuously repeats the sequence. Each bit controls its respective SAH circuit which samples the input data on the rising edge of the bit, tracks it till the falling edge, and holds it over the period from the falling edge to the next rising edge. Essentially it converts the real-time input into sampled analog data and presents it to the analog block structure. The waveforms obtained at the output of the sample and hold array after simulation are as shown in Figure 5. The input applied was a positive going ramp.

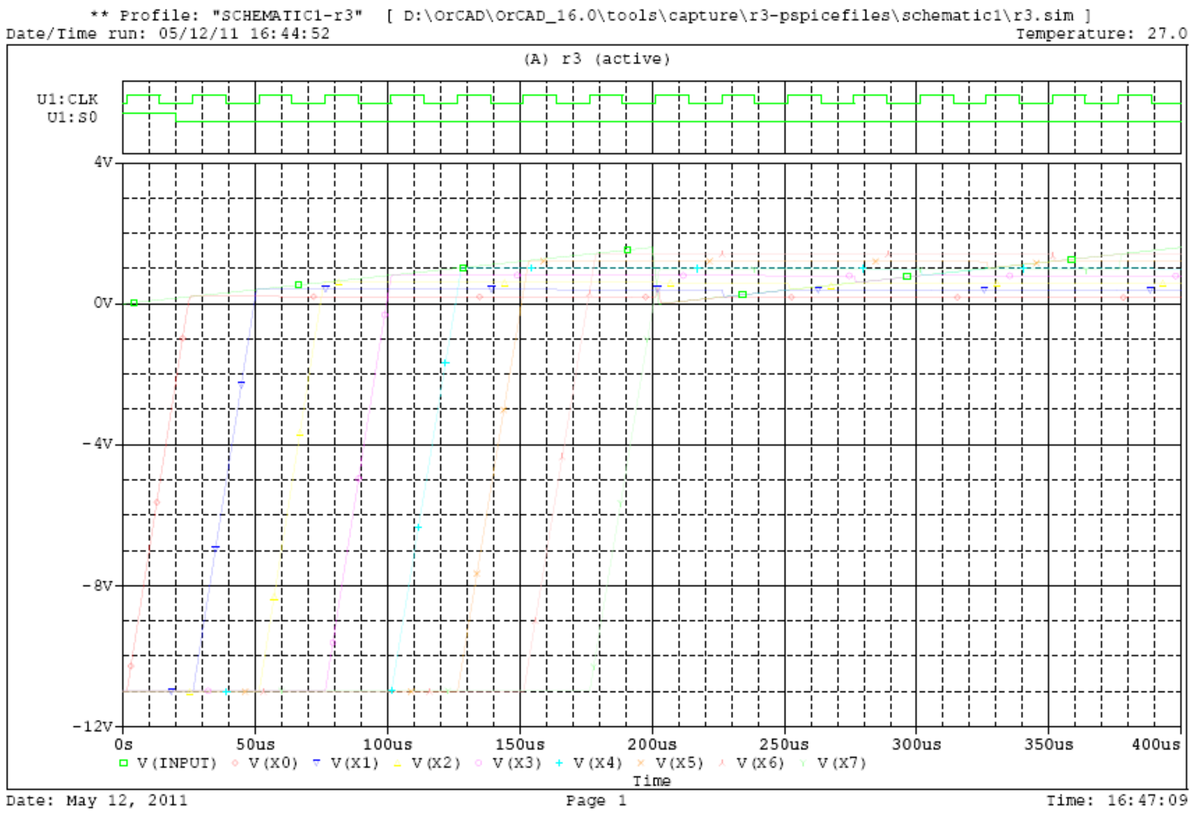


Figure 5. Waveforms obtained at the output of the sample and hold array

C. *Analog Block Structure*

The analog block structure to obtain the DHT for N = 2, 4 and 8 is shown in Fig. 6. Each butterfly in the SS is implemented by a single SAB. Each stage has $N/2$ butterflies and hence requires $N/2$ SABs to implement it. Similarly, each butterfly in the MS is implemented by a single MAB. For each stage S from 3 to P, there are $2^{(P-S)}$ MSs and each MS has $(2^{(S-2)} - 1)$ MABs. The total number of MABs for each stage are $2^{(P-S)} \cdot (2^{(S-2)} - 1)$. The analog block structure computes the DHT and makes it available at the output.

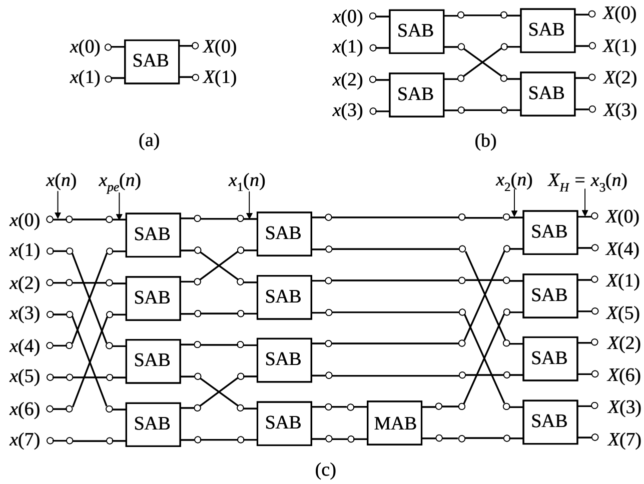


Figure 6. Analog block structure to obtain the DHT for (a) N = 2, (b) N = 4 and (c) N = 8

V. SIMULATION RESULTS

The architecture for N = 8 has been tested by simulating it with the help of Orcad PSpice. The simulation results are shown in Fig. 7.

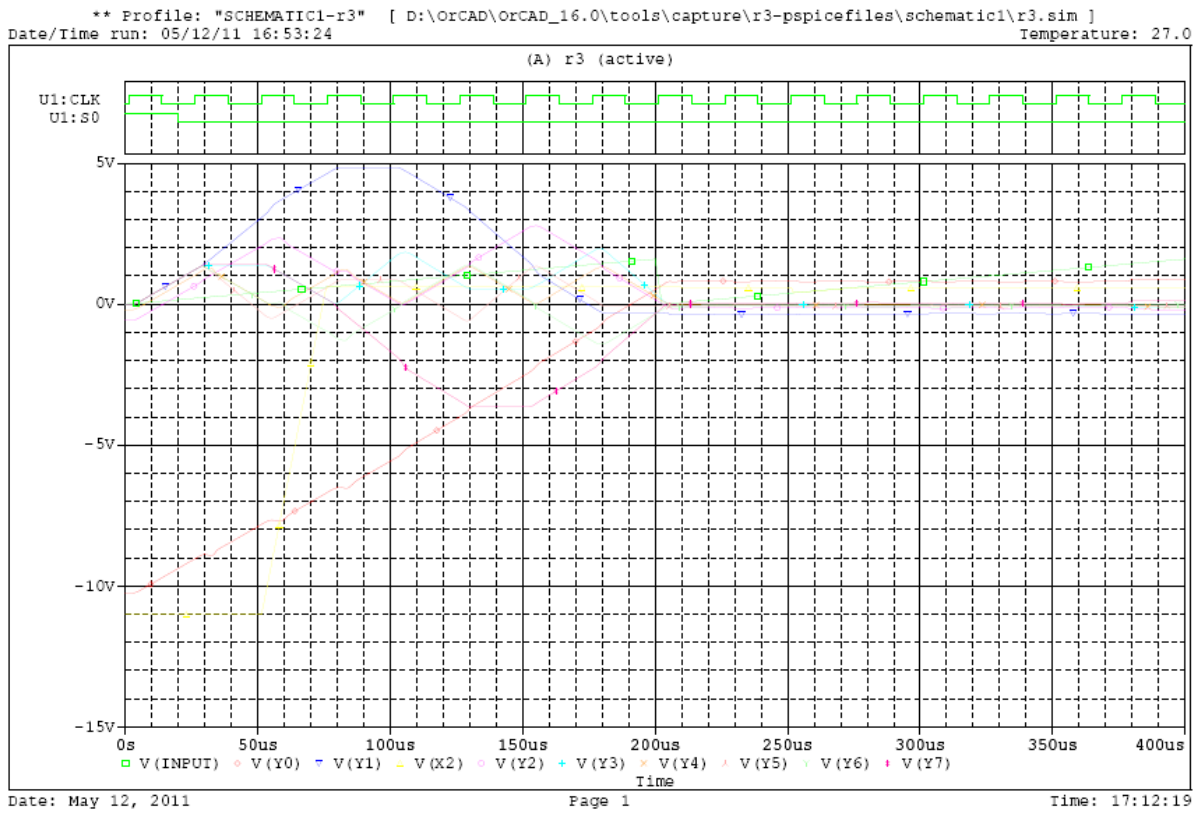


Figure 7. Waveforms obtained at the output of the Analog block structure for N = 8

The forward transformation of the DHT has been tested by applying a positive going ramp input. The ramp is sampled by the SAH array which is digitally controlled by the ring counter. The output of the SAH array forms the input sequence and is denoted as *V*(*XN*) which is applied to the analog block structure. The output sequence after the forward transformation is obtained at the output of the analog block structure and is denoted as *V*(*YN*). The theoretically calculated output values and the measurement values obtained by simulation of the forward transformation are tabulated in Table II and are in good agreement.

TABLE II. COMPARISON OF THEORETICAL VALUES AND SIMULATION RESULTS

n	**Input $x(n)$**	**Theoretical Values of output X_H**	**Simulation Results of output X_H**
0	0.2	0.900	0.890
1	0.4	-0.341	-0.349
2	0.6	-0.200	-0.201
3	0.8	-0.141	-0.139
4	1.0	-0.100	-0.099
5	1.2	-0.059	-0.060
6	1.4	0.000	0.003
7	1.6	0.141	0.139

VI. CONCLUSIONS

In the algorithms [1]-[5], the stage structures perform the additions and multiplications. The proposed algorithm introduces multiplying structures which perform all the multiplications with the cosine coefficients and their related additions. This simplifies the stage structures which now perform only the additions. The distinct advantage is that the number of multiplications is reduced without affecting the number of additions. It has been shown that the proposed analog circuit can perform both the additions and multiplications. The architecture being modular and can be scaled for large values of *N* unlike the neural net approach in [22]. The proposed architecture is a mixed-mode architecture in which the analog block structure is mixed with digital control. The real-time signal is converted into sampled analog data with the help of the SAH array. The analog block structure then processes the sampled analog data simultaneously at each stage, hence the architecture is faster than those based on the multiply and accumulate approach [26]. The architecture for the forward DHT has been tested by performing the simulation on Orcad PSpice. It can easily be modified to implement a decimation-in-frequency algorithm as well as the inverse transformation. The architecture could prove suitable for signal processing using field programmable analog arrays [27]-[28].

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