Design and Simulation for Producing Two Amplitude Matched Anti-phase Sine Waveforms Using ±2.5 V CMOS Current-Mode Approach

Anil Kumar Sharma (MIEEE)
Associate Professor, Dept. of Electronics & Comm. Engg.
Institute of Engg. & Tech., Alwar-301030, Raj., India

Dipankar Pal (MIEEE)
Professor & Principal, Deptt. of ECE
B. C. Roy Engg.College, Durgapur-713206, W.B., India.

Abstract— In this paper the current mode approach called "Current Conveyor (CCII+)" has been incorporated to design and simulate the circuit for producing two amplitude matched anti-phase sine waveforms which are frequently used in various communication and instrumentation systems. PSpice simulation has been used to depict the output waveforms. The power supply used is ±2.5 V which can be easily incorporated with CMOS IC technology. The designed circuit has been simulated at various frequency ranges and the waveforms are obtained after the circuit is optimized.

Keywords- Current Mode, PSpice, OrCAD, CCII+, CMRR, Op Amp.

I. INTRODUCTION

The sinusoidal waveform is fed to the proposed circuit which then produces two amplitude matched anti-phase (exactly 180º out of phase) sine waveforms over a large frequency range with a gain factor of unity. The characteristics of the circuit make it suitable for various applications like balanced signal transmission of analog signals in the presence of unwanted common-mode voltages, lock-in-based systems to eliminate the effects of offset, synchronous detection [2], phase comparator circuits [3] and bridge measuring circuits for increasing the sensitivity of bridge circuits such as a Wheatstone bridge [4]. For its realization in the beginning a very simple and common approach was given by Golnabi and Ashrafi [4] as shown in Fig.1.

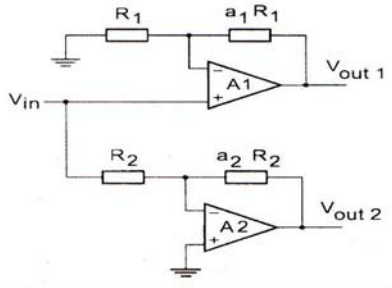

Fig. 1: Circuit of Golnabi and Ashrafi [4].

But this circuit has few disadvantages: (i) The gain for both the outputs are different as the closed loop gain of amplifiers A_1 and A_2 are $(1+a_1)$ and $(-a_2)$ respectively as mentioned by Baert [3]. (ii) It has a small gain-bandwidth product due to the use of conventional voltage-mode operational amplifier. (iii) This circuit demands the precise matching of the poles of the amplifiers if a low error is to be required (The transistor should be perfectly matched). Baert [3] has discussed another circuit as shown in Fig. 2, which exhibits an improvement in the performance of the previous circuit in that it has closed loop gains of the two amplifiers equal to one. If required a gain factor can be achieved by amplification of the output voltages V_{out-1} and V_{out-2} with the help of matched amplifier circuits. Thus in this circuit both the parameters i.e. 180^0 phase inversion and the amplification functions are separated and a wide bandwidth can be achieved. But the limitations of the circuits are precise matching of the poles of the amplifiers for achieving low error and the restricted gain.

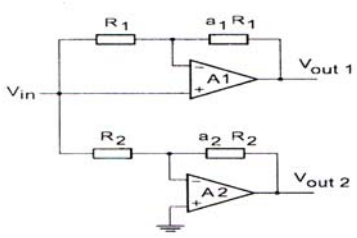

Fig. 2: Circuit of Baert for Generating the Antiphase Signals. [3]

In order to further improve the performance of the existing systems a new scheme was introduced by Gift [2]. This circuit has the advantages of large frequency range of operation, not requiring the precise matching of the amplifier poles, also it does not have any gain restriction, which was a critical requirement of the circuit of Baert. This circuit is designed with the help of two operational conveyors (OCs). An OC is a block structured device consisting of an Op. Amp.

and a second-generation current conveyor, CCII+ as shown in Fig.3.

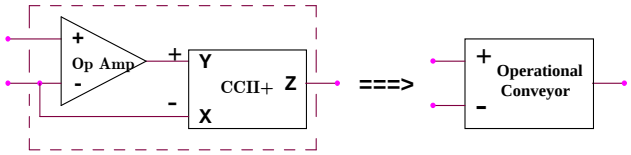

Fig. 3: OC Consisting of an Op-Amp and a CCII+

In this circuit the feedback loop of the op-amp, consists of the input circuit (Port-X and Port-Y) of the current conveyor. The effect of this is the virtual elimination of the resistor seen at the inverting input of the current conveyor so that the current through this component is fully determined by external components and the input voltage. This technique gives a well-defined system transfer function.

II. Proposed Circuit

The basic structure of the proposed model is presented in Fig. 4. It consists of two op. amps. working in combination with two CCII+, two-grounded loads (R_L), a current and gain determining resistor (R_G), and the two feedback loops around the operational amplifiers. The input circuit of the CCII+ forms a part of the feedback loop of the op. amp. This results in virtual elimination of the register seen at the inverting input of the CCII+, so that the current through this component is fully determined by external components and the input voltage.

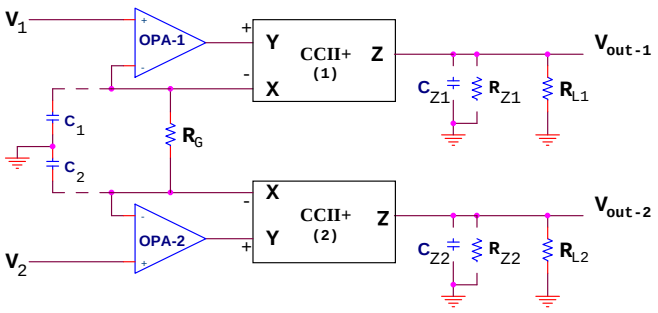

Fig. 4: Proposed Model for producing two Amplitude Matched Anti – phase Sine waveforms

This technique gives a well-defined system transfer function. In this Fig.4 the two sets, each consisting of an op amp with a CCII+, are arranged in a differential-input mode and the output signal currents (which are equal and anti-phase) are flowing into the resistors R_{L1} and R_{L2}. The input signals V_1 and V_2 are applied at the non-inverting terminals of the op amps and the two inverting terminals are connected through a resistor R_G called the gain setting resistor. C_1 and C_2 are the parasitic capacitances at the inverting inputs while R_{Z1}, C_{Z1} and R_{Z2}, C_{Z2} are the respective output impedance parameters. For using the circuit in single-ended input-mode, one of the input terminal (say V_2) is grounded. As per definition and internal construction of the ideal CCII+, V_X should be equal to V_Y and I_Z be equal to I_X. However in actual operation an error ϵ_V (voltage transfer error) occurs in transferring the voltage from terminal Y to X, as well as ϵ_C (current transfer error) due to the action of CCII+ component in transferring the current from terminal Z to X [5,6,7]. Hence we can write

$$V_{X1}=V_{Y1}(1-\epsilon_{V1})=V_1(1-\epsilon_{V1}) \quad (1)$$

$$V_{X2}=V_{Y2}(1-\epsilon_{V2})=V_2(1-\epsilon_{V2}) \quad (2)$$

$$I_{Z1}=I_{X1}(1-\epsilon_{C1}) \quad (3)$$

$$I_{z2}=X_2(1-\epsilon_{C2}) \quad (4)$$

The phase difference ($\Delta\Phi$) of the output signal can be calculated as:

$$\Delta\Phi = \tan^{-1}(\omega C_1 R_G)-\tan^{-1}(\omega C_{Z1} R_{L1}) -\tan^{-1}(\omega C_{Z2} R_{L2})+180^0 \quad (5)$$

and

$$f_T=1/2\pi C_1 R_G \quad (6)$$

Hence we can conclude that the amplitude difference between the two output signals (V_{out-1} & V_{out-2}) increases with frequency and the phase shift between them can only be minimized by keeping the value of R_G as low as possible.

III. Software Used

Most of the simulators are based on various versions of SPICE (Simulation Program with Integrated Circuits Emphasis). PSpice is THE choice of professionals for simulation. "PSpice is the de facto standard for analog and mixed-signal simulation... includes a powerful and robust simulation engine and works with Orcad Capture or PSpice Schematics in an integrated environment. In this project the Simulation and Analysis of the circuit has been carried out mainly with the help of OrCAD 10.0 software. The name OrCAD is a portmanteau, reflecting the software's origins: Oregon + CAD. The OrCAD is a software tool produced by “Cadence Design Systems” for electronic design automation.

IV. Circuit Design and Simulation

First of all we have designed and verified the CMOS two stage un-buffered Op amp as shown in Fig.5.

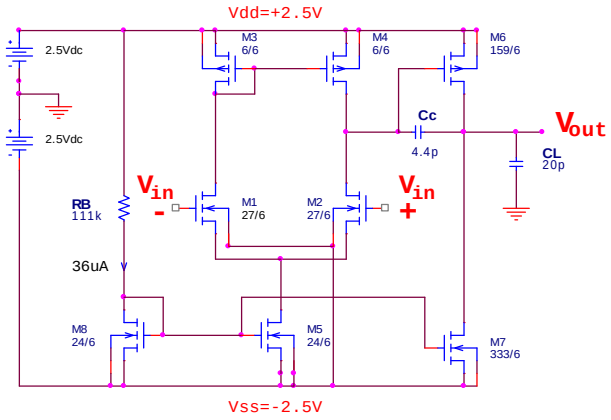

Fig. 5: CMOS Two Stage Un-buffered Op-Amp

After this circuit is verified it can be used further to construct a unity gain voltage buffer, which will be used in the implementation of the RC sine waveform circuit with variable frequency. Later its signal output will be fed to the balanced output signal circuit. The aspect ratio (W/L) parameter of all the transistors from M1 to M7 has been calculated as mentioned in table 1. Transistor M8 is used to provide the biasing.

Table 1: Transistor Dimensions of Two Stage Op. Amp.

Transistors	Aspect ratio W (µm)/L (µm)
M1- M2	27/6
M3- M4	6/6
M5	24/6
M6	159/6
M7	333/6
M8	24/6

In Fig. 6 we have shown the schematic of a CMOS voltage buffer derived from the already made op amp mentioned in Fig. 5. The input transconductance stage provides high input impedance and is the major contributor to the op amp dc gain while the output stage determines output impedance; output voltage swing and the powered delivered to the load.

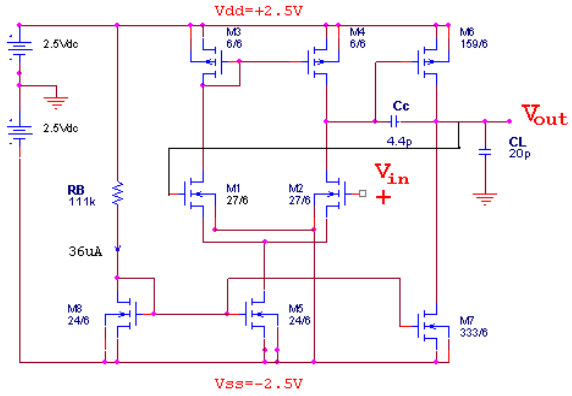

Fig. 6: Schematic of the CMOS Voltage Buffer

The circuit is simulated with Pspice and the results were found very satisfactory. In the simulation we checked the circuit by feeding a sine waveform signal of 1volt amplitude with a frequency of 1MHz. The R_L was taken as 12 K. The input and output waveforms were found perfectly matched in amplitude as well as in phase as shown in Fig. 8.

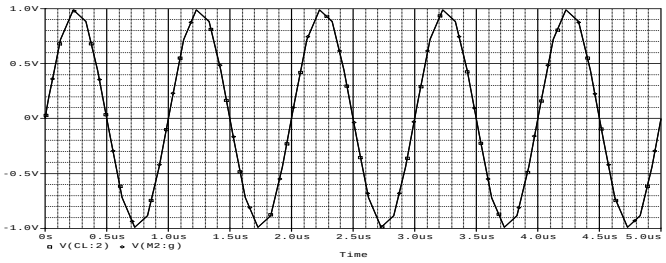

Fig. 7: Response of the CMOS Unity Gain Buffer to a Sine waveform Signal at 1MHz

The circuit schematic of the CMOS CCII+ is shown in Fig. 8. It uses ± 2.5V supply for Vdd and Vss respectively and an external resistor R1 for proper biasing which gives a bias current of 25µA [9]. The complete proposed circuit using CMOS CCII+ is shown in Fig. 9

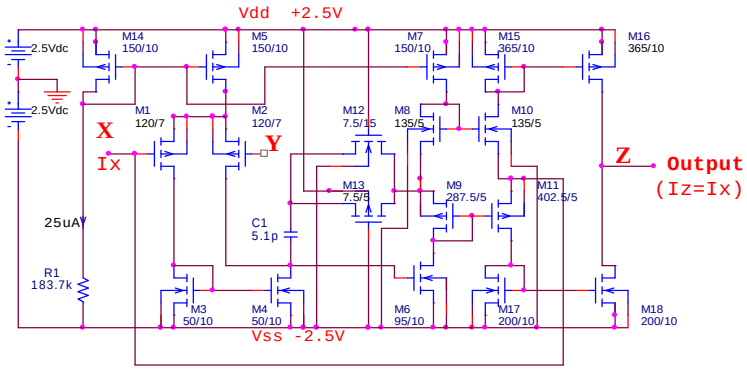

Fig. 8: Circuit Schematic of CMOS CCII+

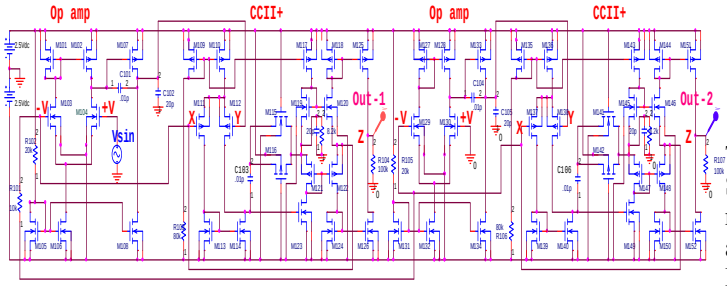

Fig. 9: The Proposed Circuit Using CMOS CCII+

Case-1: The sine waveform outputs (V_{out-1} and V_{out-2}) with the input sine waveform signal at frequency 34 MHz are shown in Fig. 10. Both the outputs are perfectly balanced and exactly Anti-f phase as expected.

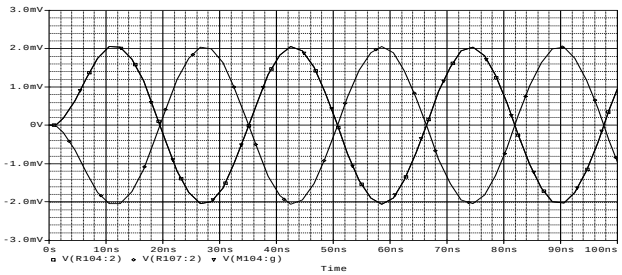

Fig. 10: The Simulated Balanced Output Waveforms at 34 MHz with input waveform.

Case-2: The sine waveform outputs at maximum frequency of 98 MHz are shown in Fig. 11.

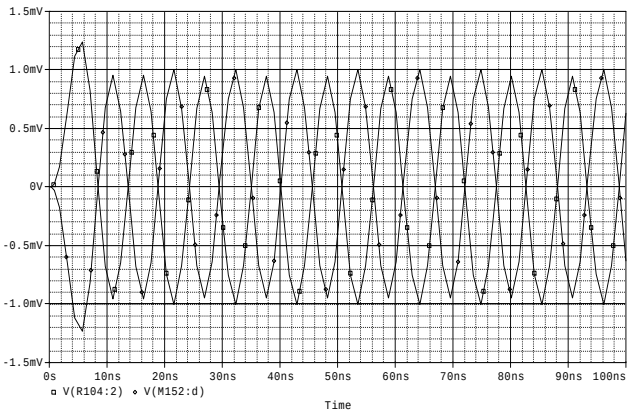

Fig. 11 : The Simulated Balanced output Waveforms at Frequency 98 MHz With input waveform

V. Conclusion

The CMOS CCII+ based circuit for producing two anti-phase Sine waveforms has been simulated successfully and the results are found satisfactory. The accurate amplitude matched antiphase signals are produced upto the frequencies of 84 MHz without using any matched devices. Above this frequency and upto the 98 MHz, the two outputs are little distorted, in that the amplitudes of the first half cycles of the two waveforms are bit exceeding than their sustained output voltages, otherwise both the waveforms are perfect and without the loss of significant gain. The main advantage of the circuit is the use of CMOS CCII+ instead of conventional op. amp. with the present trend towards the design of current-mode circuits and because the ground capacitors structures are compatible with the CMOS technology, the proposed conFiguration will be more suitable for adaption to monolithic IC form. The circuit can provide the voltage as well as the current outputs.This circuit also does not require the precise matching of the amplifier poles. Changing the resistance RG connected between the two negative terminals of the OC1 and OC2 can vary the gain of the circuit. The performance is superior to the previously discussed circuits by Golnabi [3], Baert [2] and Gift [1], where the maximum frequency of operation was limited upto 400KHz, 1.5 MHz and 1 MHz respectively and here the frequency range is upto 98 MHz.

VI. Future Scope

The further work can be taken up to increase the frequency in the order of GHz. and removal of the distortions produced in the first half cycle at 98 MHz, also the work can be extended to verified the circuit for other waveforms like square, triangular, ramp, pulse, exponential etc, and to implement the whole circuit into a single IC/chip using CMOS design technology.

REFERENCES

[1] Falconi, C. Ferri, G. Stornelli, V. De Marcellis,A. Mazzieri, D. D'Amico A, "Current-Mode High Accuracy High Precision CMOS Amplifiers," IEEE Trans. On Circuits and Systems, 2008, 55(5): pp. 394-398.

[2] Stephan J. G. Gift and Brent J. Maundy, "Balanced-Output-Signal Generator," IEEE Trans. Instrum. Meas.,2006, 55(3): pp 835-838.

[3] Daniel Henri Jean Baert, "Circuit for the Generation of Balanced Output Signals," IEEE Trans. Instrum. Meas., 1999, 48(6): pp. 1108-1110.

[4] Hossein Golnabi and Ashkan Ashrafi, "Producing 180º Out-of-Phase Signals From a Sinusoidal Waveform Input," IEEE Trans. Instrum. Meas., 1996, 45(1): pp. 312-314.

[5] Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design," 2nd Edition. Oxford Univ. Press, New York, 2002.

[6] A.S. Sedra, G.W. Roberts, and F. Gohh, "The Current Conveyor: History, Progress and New Results," IEE Proceedings-G, 1990, 137(2), pp. 78-87.

[7] Yehya H. Ghallab, Wael Badawy, Karan V.I.S. Kaler, and Maundy B.J., "A Novel Current-Mode Instrumentation Amplifier Based on Operational Floating Current Conveyor," IEEE Trans. Instrum. Meas., 2005, 54950: pp.1941-1949.

[8] Sedra A.S. and Roberts. G.W., "Current Conveyor Theory and Practice in Analogue IC design: The current-mode approach," by Toumazou C., Lidgey F.J., Haigh D.G.(Eds.). London, Peter Peregrinus Ltd.,1998. Chap-3, pp. 93-126.

[9] Sedra A. and Smith K.C., "Second-Generation Current Conveyor and Its Applications," IEEE Trans. on Circuit Theory,1970, CT-17, pp. 132-134.

[10] Anwar A. Khan, Sadanand Bimal, Dey K.K. and ROY S. S., "Novel RC Sinusoidal Oscillator Using Second Generation Current Conveyor," IEEE Trans. Instrum. Meas., 2005, 54(6), pp.2402-2406.

[11] Baker R. J., Harry W. Li, David E. Boyce, "CMOS Circuit Design, Layout, and Simulation," IEEE Press Series on Microelectronic Systems. Prentice Hall of India Pvt. Ltd. New Delhi, 2005.

Anil Kumar Sharma (MIEEE) received his M.E. degree in Electronics and Communication Engineering from Birla Institute of Technology, Deemed University, Mesra, Ranchi – India, in 2007 with first division (CGPA of 8.45 in a 10.00-point scale). He has an experience of 20 years on various RADARs and Communication Equipments. He is currently an Associate Professor in the Department of Electronics and Communication Engineering, Institute of Engineering and Technology, Alwar- 301 030, Rajasthan, India. He has published 16 papers in International journals as well as in international and national conferences. His research and teaching interest include Microprocessor, VLSI Design, Neuro-Fuzzy Modeling , RADARs & its Data Handling Systems.

Dipankar Pal (MIEEE) received his B. Tech (Electrical Engineering) from IIT Delhi and did his Ph. D. at the Dept. of Electronics & Telcommunication Engineering, Jadavpur University. He has done postdoctoral at UCL, London and then at the University of Bath (UK). He is presently the professor and Principal, B. C. Roy Engineering College, Durgapur, West Bengal-713206, India. He has published over 40 papers in international and national journals as well as in international and national conferences. His research interests include Microelectronics, ASIC & VLSI Design, Embedded Systems, Biomedical Electronics.