Performance evaluation of H.264 decoder on different processors

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***Abstract*---H.264/AVC (Advanced Video Coding) is the newest video coding standard of the moving video coding experts group. The decoder is standardized by imposing restrictions on the bit stream and syntax, and defining the process of decoding syntax elements such that every decoder conforming to the standard will produce similar output when encoded bit stream is provided as input. It uses state of art coding tools and provides enhanced coding efficiency for a wide range of applications, including video telephony, real-time video conferencing, direct-broadcast TV (television), blue-ray disc, DVB (Digital video broadcast) broadcast, streaming video and others. The paper proposes to port the H.264/AVC decoder on the various processors such as TI DSP (Digital signal processor), ARM (Advanced risk machines) and P4 (Pentium processors). The paper also proposes to analyze and compare Video Quality Metrics for different encoded video sequences. The paper proposes to investigate the decoder performance on different processors with and without deblocking filter and compare the performance based on different video quality measures.**

Keywords- H.264; decoder; processors; deblocking filter; macro blocks

I. INTRODUCTION

Digital video compression techniques have played a key role in recent multimedia communications. The limitation of bandwidth in communication channels and storage media demands more efficient video coding methods. Introducing new applications and advances in multimedia technology demands video coding methods to include more complex and advanced features. Compression is the process of compacting data into a smaller number of bits. Video compression (video coding) is the process of compacting or condensing a digital video sequence into a smaller number of bits. Compression involves a complementary pair of systems, a compressor (encoder) and a decompressor (decoder). The encoder converts the source data into a compressed form (occupying a reduced number of bits) prior to transmission or storage and the decoder converts the compressed form back into a representation of the original video data. The encoder/decoder pair is often described as a *CODEC* (en*CO*der/ *DEC*oder). H.264 decoder complexity is higher on the encoder side and on the decoder side, the complexity is estimated to be two to three times higher than an H.263 decoder for the same bit rate [1]. Several studies examined H.264/AVC decoder performance on a general purpose processor [1]-[4]. The paper describes a comparative work which examines H.264/AVC decoder performance on three processors.

A baseline profile version is used for experimentation and the purpose of the paper is to examine the performance in terms of video quality measurements on different processors. The paper also investigates the performance of the decoder on different processors with and without the use of deblocking filter.

The paper is organized as follows. Section 2 gives overview of H.264 decoder, section 3 gives overview of processors. session 4 discusses the comparison parameters, the implementation details and test results are discussed in section 5 and 6. Finally conclusions are drawn.

II. H.264 DECODER

OVERVIEW OF H.264 DECODER

The decoder receives a compressed bit stream from the NAL (network abstraction layer). The data elements are entropy decoded and reordered to produce a set of quantized coefficients. These are rescaled and inverse transformed and using the header information decoded from the bit stream, the decoder creates a prediction macro block identical to the original prediction formed in the encoder.

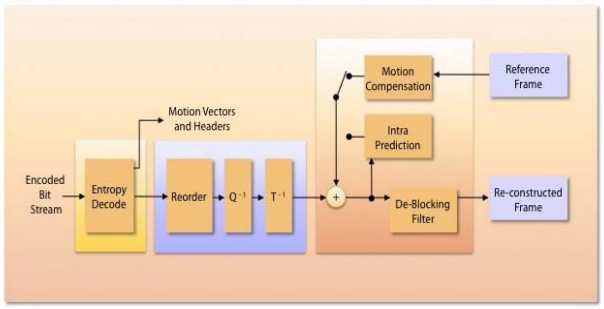

Figure1: Block diagram of H.264

DEBLOCKING (LOOP) FILTER

H.264 uses an adaptive de-blocking filter that operates on the horizontal and vertical block edges within the prediction loop in order to remove artifacts caused by block prediction errors[13]. The filtering is generally based on 4x4 block boundaries, in which two pixels on either side of the boundary may be updated using a different filter. The filter smoothens block edges, improving the appearance of decoded frames. The filtered image is then used for motion-compensated prediction of future frames. The inclusion of deblocking filter before motion compensated prediction stage is beneficial in terms of compression efficiency.

Figure 2 illustrates the principle of the deblocking filter. Whether the samples p_0 and q_0 as well as p_1 and q_1 are filtered

is determined using quantization parameter (QP) dependent thresholds α (QP) and β(QP).

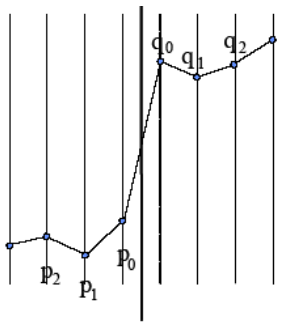

Figure 2: Principle of deblocking filter

Filtering of p_0 and q_0 only takes place if each of the following conditions is satisfied:

1. $|p0 - q0| < \propto (QP)$
2. $|p1 - p0| < \beta(QP)$
3. $|q1 - q0| < \beta(QP)$

Where β (QP) is considerably smaller than α (QP).

Filtering of p_1 or q_1 takes place if

$$|P2 - P0| < \beta(QP) \quad or \quad |q2 - q0| < \beta(QP)$$

If a relatively large absolute difference between samples near a block edge is measured, blocking artifact should be reduced. However, if the magnitude of that difference is so large that it cannot be explained by the coarseness of the quantization used in the encoding, the edge is more likely to reflect the actual behavior of the source picture and should not be smoothed over.

III. OVERVIEW OF THE PROCESSOR

There are many factors one has to take into account when considering the implementation of H.264 decoder on processors. The parameters considered can be speed, memory, cost, size, power consumption, etc. The paper proposes to consider the parameters such as MSE (mean square error), PSNR (peak signal to noise ratio), SSIM (structural similarity index measure) and MSAD (mean square absolute difference) for the comparison of the three considered processors.

ARM based single board computer (ARM 920T) considered is an excellent choice for low cost, embedded development and is supported by Linux and the GNU tool chain. The GNU compiler can be used under windows based systems. The DM 642 evaluation module (EVM) is a low cost high performance video & imaging development platform designed for application development and evaluation of multi channel, multi-format digital and other future proof applications. TMS320C64x DSP core (TMS320DM642) is considered for implementing the H.264 decoder.

IV COMPARISON PARAMETERS

The H.264 decoder is implemented on the different processors and comparison is done based on different parameters. The parameters considered for comparison are MSE, PSNR, MSAD and SSIM

1. PSNR: Peak Signal to Noise Ratio (PSNR) is measured on a logarithmic scale and depends on the mean squared error (MSE) of between an original and an impaired image or video frame. $PSNR = 10\log_{10}\frac{(2^n-1)^2}{MSE}$

2. MSE: The Mean Square Error measures the difference between the frames which is usually applied to Human Visual System. It is based on pixel-pixel comparison of the image frames.
$$d(X,Y) = \frac{\sum_{i=1,j=1}^{m,n}\left(X_{i,j} - Y_{i,j}\right)^2}{mn}$$

3. SSIM: The SSIM metric is based on the evaluation of three different measures, the luminance, contrast, and structure comparison measures which are computed as
$$l(x,y) = \frac{2\mu_x\mu_y + C_1}{\mu_x^2 + \mu_y^2 + C_1}$$
$$C(x,y) = \frac{2\sigma_x\,\sigma_y + C_2}{\sigma_x^2 + \sigma_y^2 + C_2}$$
$$s(x,y) = \frac{\sigma_{xy} + C_3}{\sigma_x\sigma_y + C_3}$$
Given the above measures the structural similarity can be computed as
$$SSIM(x,y) = [l(x,y)]^{\propto}.[C(x,y)]^{\beta}.[s(x,y)]^{\gamma}$$

4. MSAD: is the mean absolute difference of the color components in the correspondent points of image. This metric is used for testing codec's and filters.
$$d(x,y) = \frac{\sum_{i=1,j=1}^{n,}|X_{i,j} - Y_{i,j}|}{n^2}$$

V. IMPLEMENTATION DETAILS

The H.264 decoder is implemented on TI DSP TMS320 DM642 operating at 600 MHz, ARM 9 processor ARM920T operating at 180 MHz and Pentium 4 processor operating at 1.5 GHz. The different video inputs are considered for the experimentation. The experimentation is done with and without deblocking filter. The sample result is displayed for further discussion.

1. Sequence title	: Akiyo
Resolution	: 176x144
Number of frames	: 150
Color space	: YUV 4:2:0
Frames per Second	: 30
Source	: Uncompressed progressive

Figure 3: Akiyo sequence, frame 100

2. Sequence title : Foreman
Resolution : 176x144
Number of frames : 150
Color space : YUV 4:2:0
Frames per Second : 30
Source : Uncompressed progressive

Figure 4: Foreman sequence, frame 11, Frame 135

3. Sequence title : Mobile
Resolution : 176x144
Number of frames : 150
Color space : YUV 4:2:0
Frames per Second : 30
Source : Uncompressed progressive

Figure 5: Mobile sequence, Frame 90

4. Sequence title : News
Resolution : 176x144
Number of frames : 150
Color space : YUV 4:2:0
Frames per Second : 30
Source : Uncompressed progressive

Figure6: News sequence, frame 20

5. Sequence title : Suzie
Resolution : 176x144
Number of frames : 150
Color space : YUV 4:2:0
Frames per Second : 30
Source : Uncompressed progressive

Figure7: Suzie sequence, Frame 40

VI. TEST RESULTS AND CONCLUSIONS

Table 1: MSE plot with and without deblocking filter on TI processor

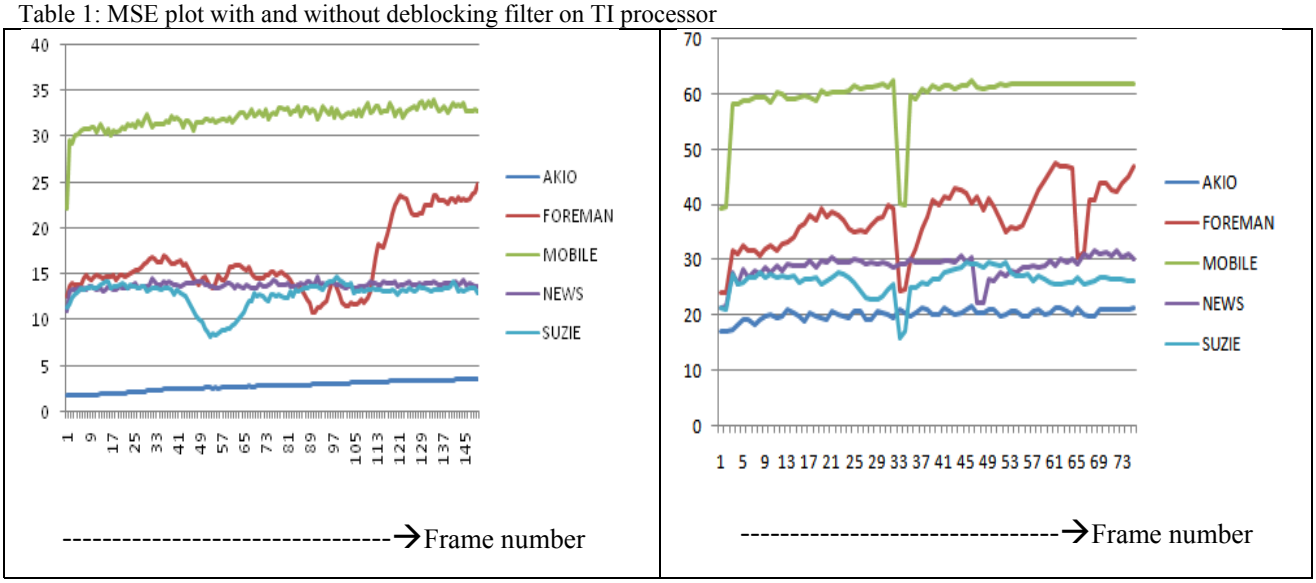

Table 2: MSE plot with and without deblocking filter on ARM processor

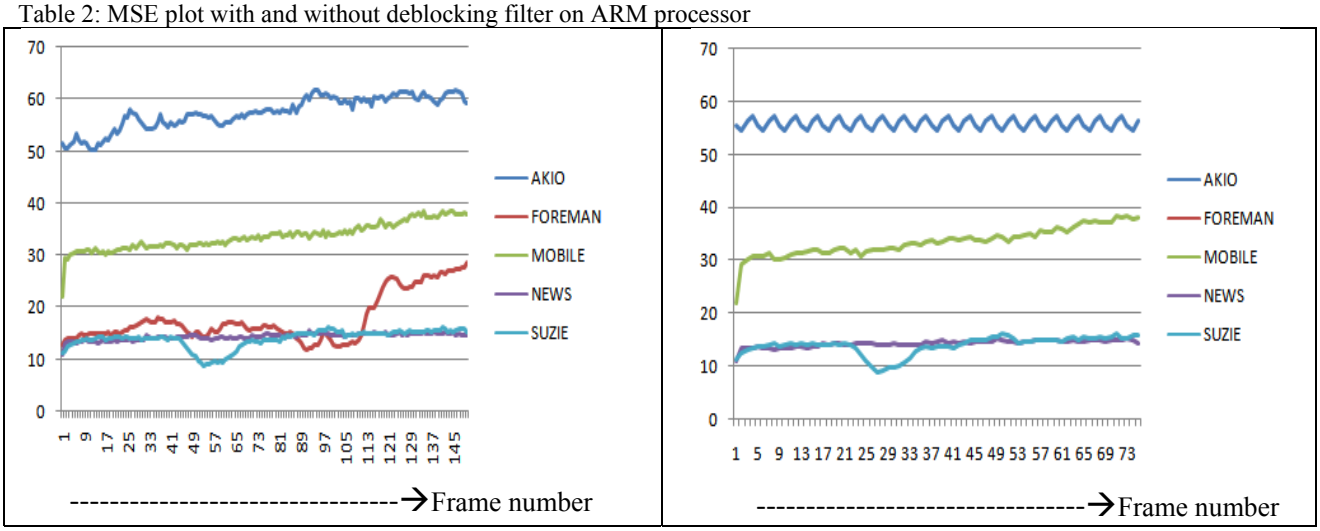

Table 3: MSE plot with and without deblocking filter on Pentium processor

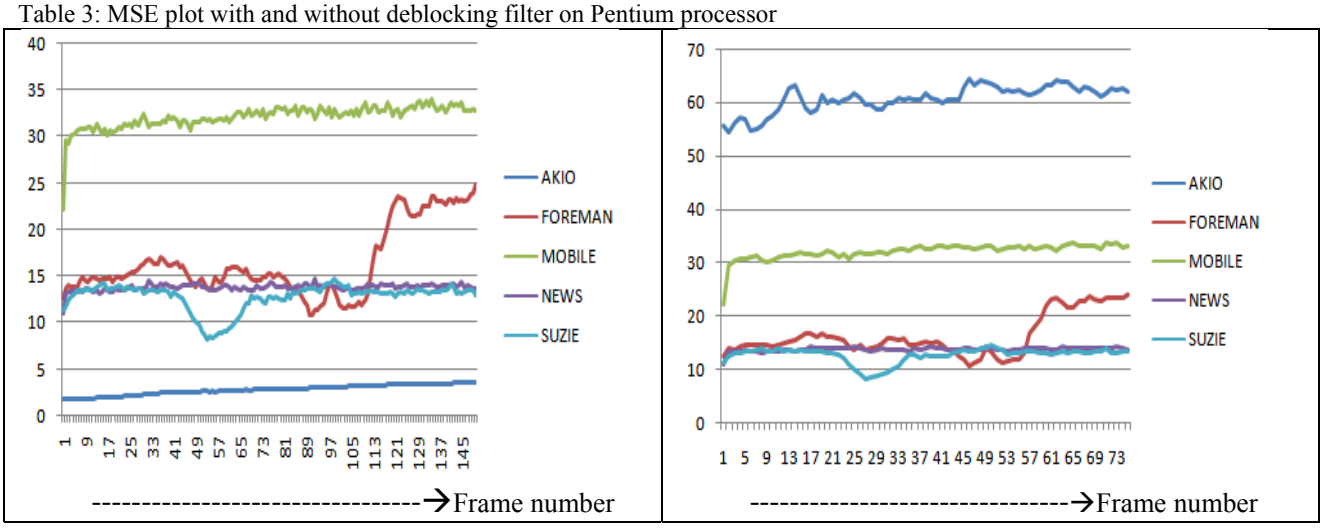

Table 4: PSNR plot with and without deblocking filter on TI processor

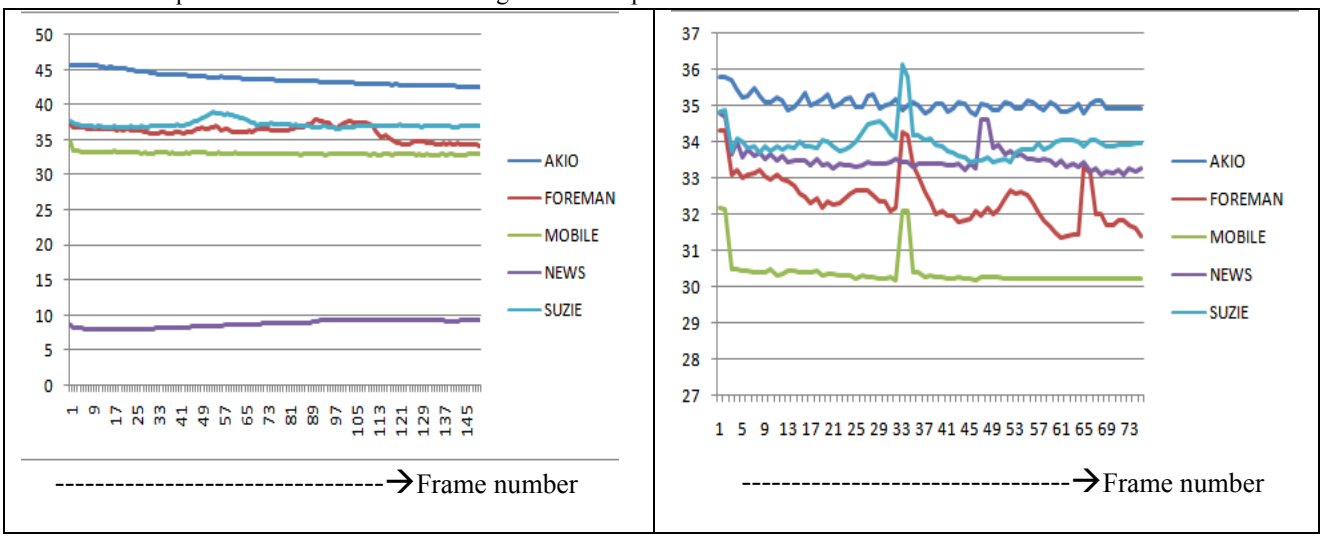

Table 5: PSNR plot with and without deblocking filter on ARM processor

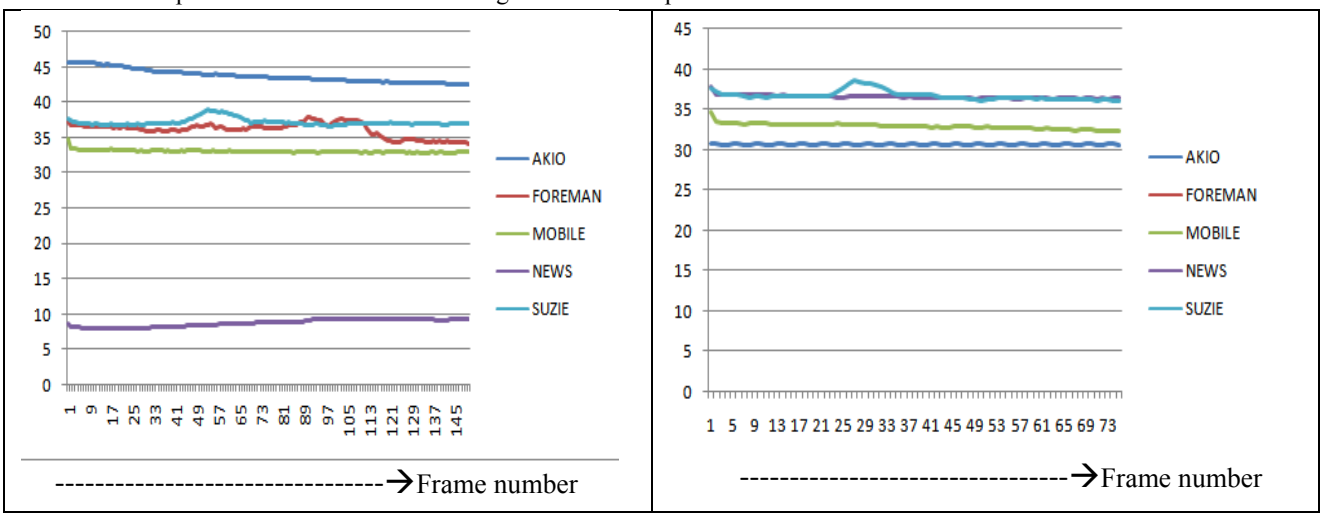

Table 6: PSNR plot with and without deblocking filter on Pentium processor

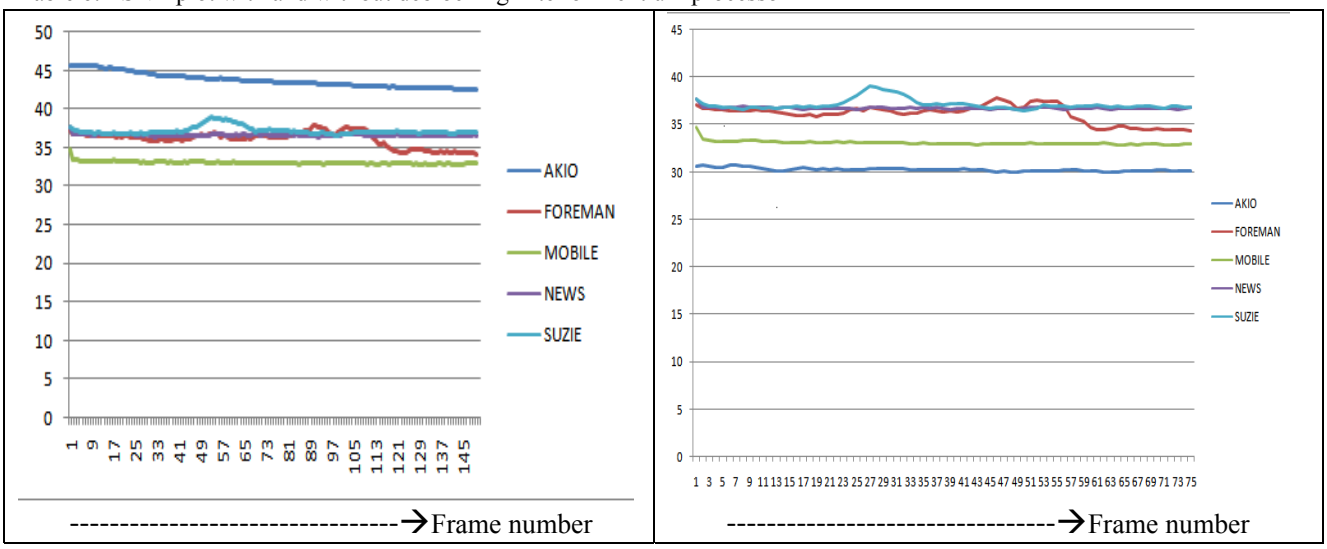

Table 7: MSAD plot with and without deblocking filter on TI processor

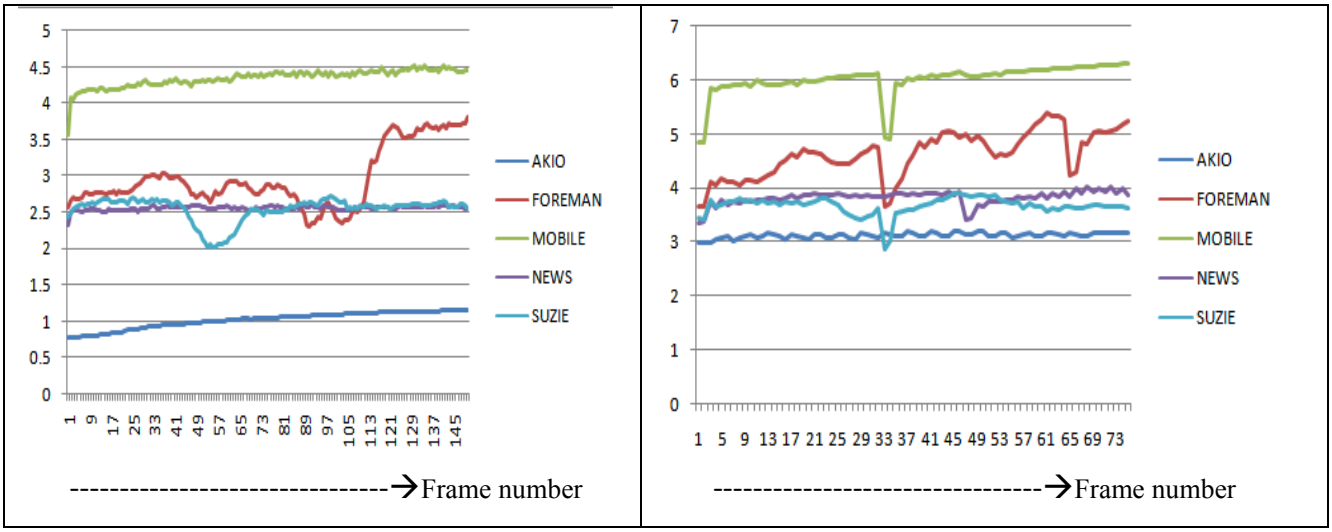

Table 8: MSAD plot with and without deblocking filter on ARM processor

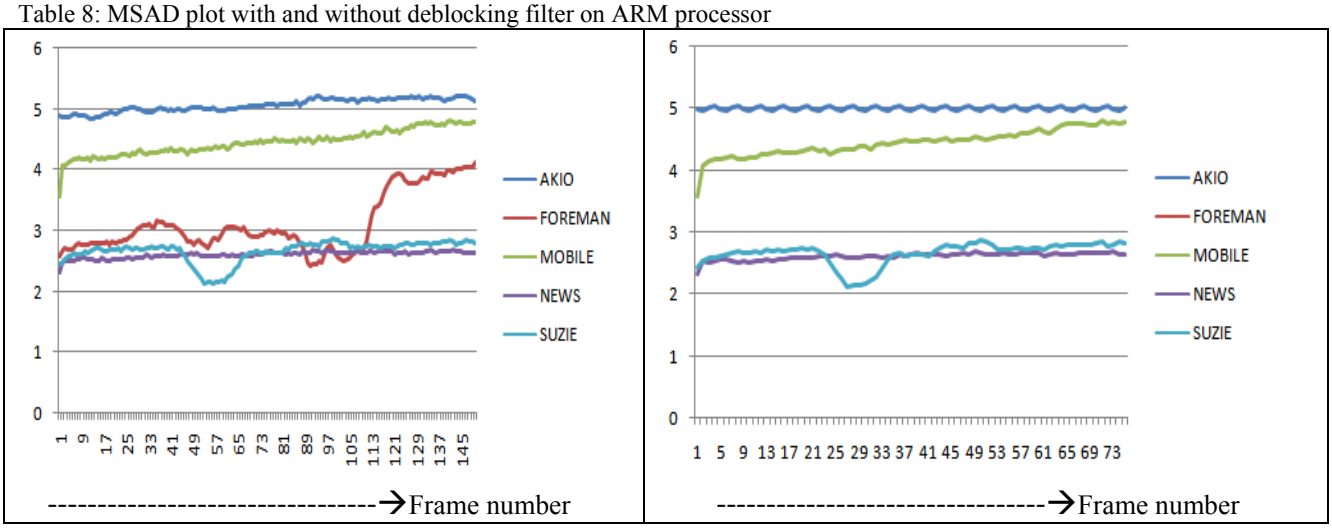

Table 9: MSAD plot with and without deblocking filter on Pentium processor

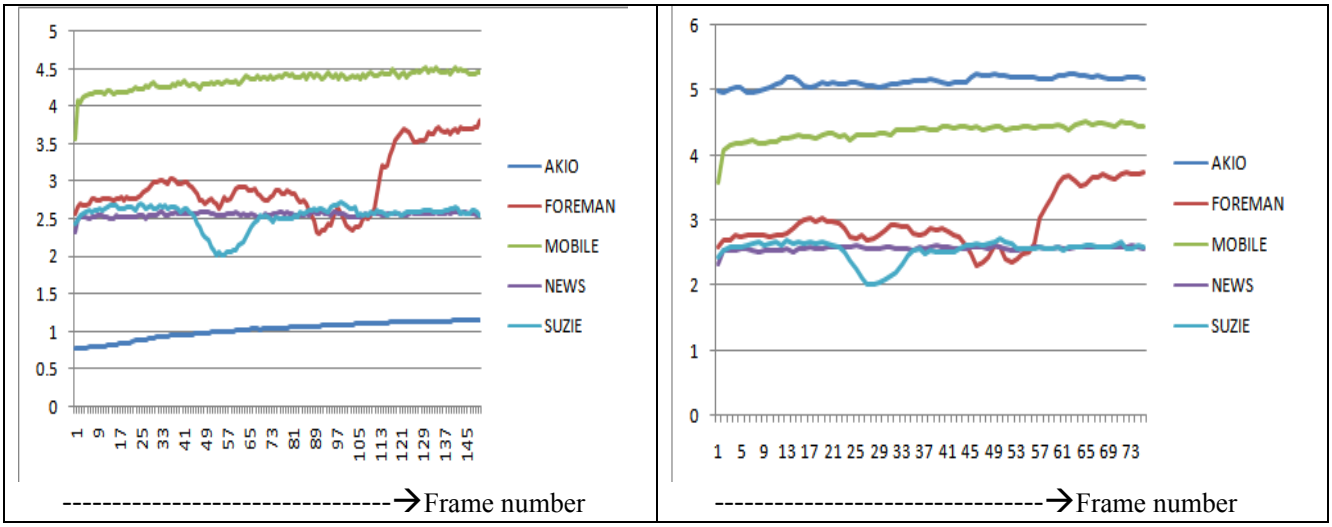

Table 10: SSIM plot with and without deblocking filter on TI processor

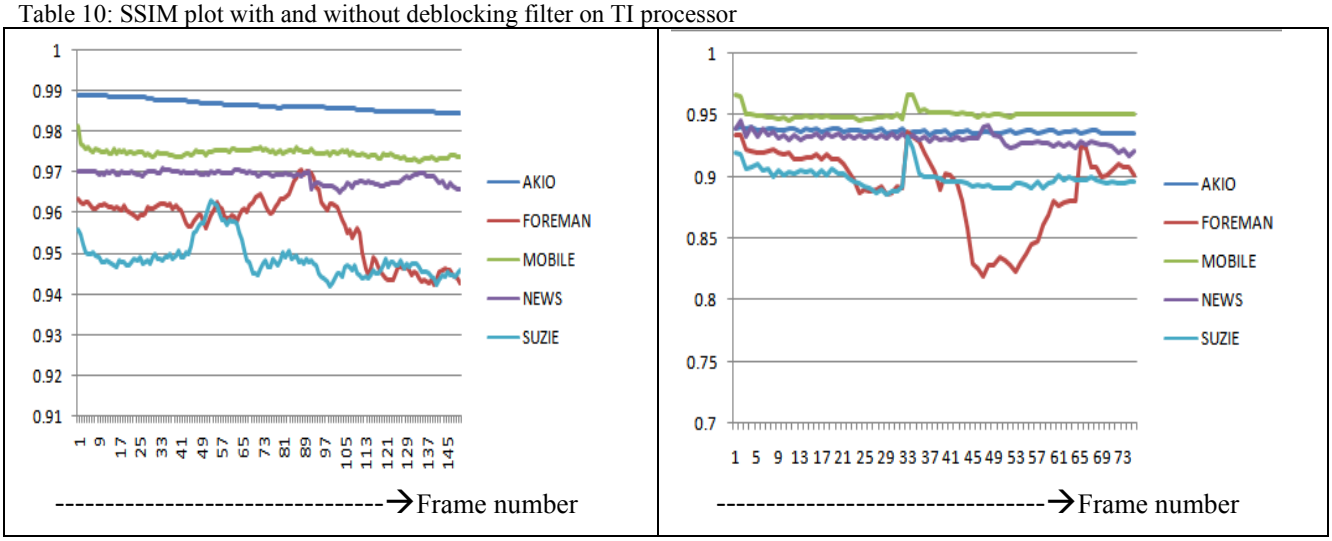

Table 11: SSIM plot with and without deblocking filter on ARM processor

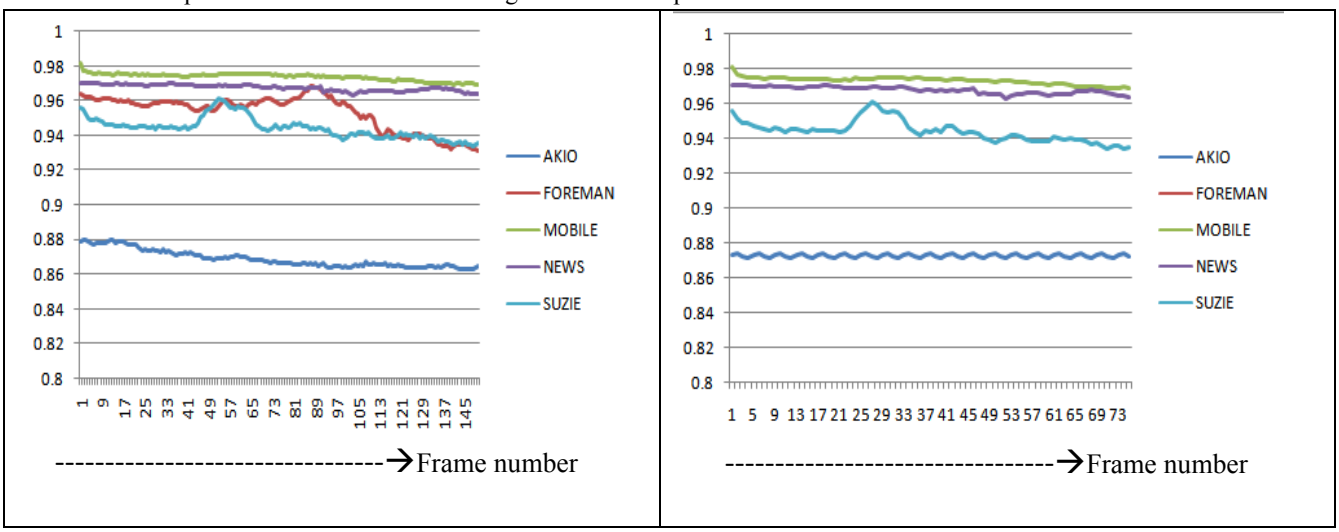

Table 12: SSIM plot with and without deblocking filter on Pentium processor

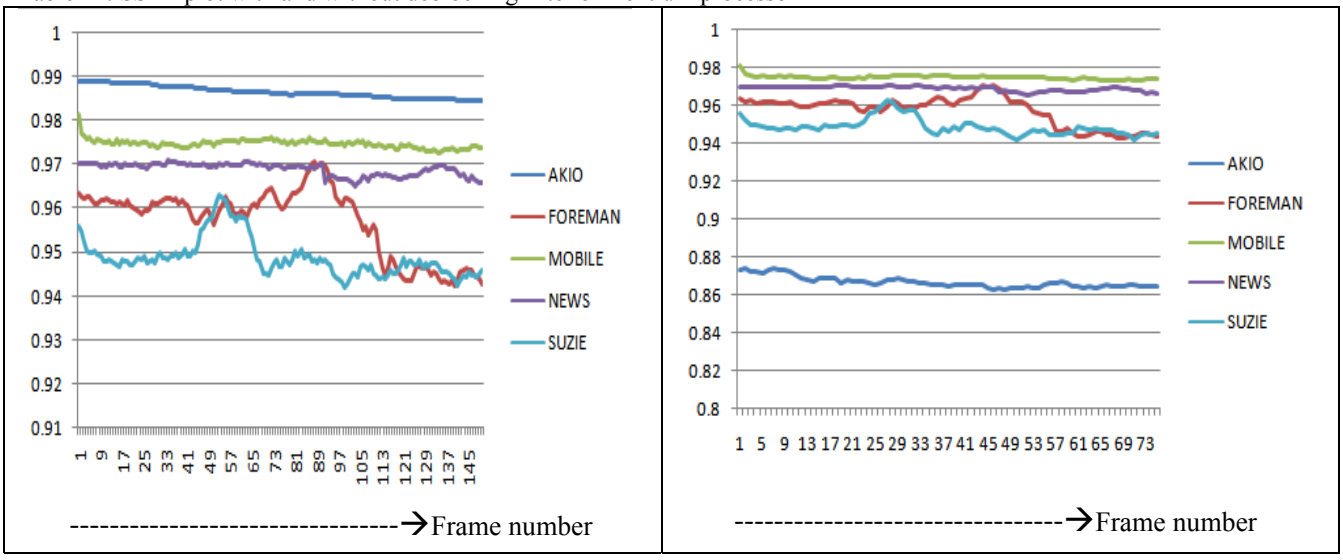

Table 13: Video quality measures on H 264 decoder with deblocking filter for encoded stream akiyo

Frame number	MSE			PSNR			SSIM			MSAD		
	TI	ARM	P4	TI	ARM	P4	TI	ARM	P4	TI	ARM	P4
1	1.75	51.51	1.75	45.70	31.01	45.70	0.99	0.88	0.99	0.79	4.88	0.79
11	1.79	50.54	1.79	45.60	31.09	45.60	0.99	0.88	0.99	0.81	4.85	0.81
21	1.96	53.30	1.95	45.21	30.86	45.21	0.99	0.88	0.99	0.86	4.93	0.86
31	2.30	54.95	2.29	44.	30.73	44.52	0.99	0.87	0.99	0.93	4.98	0.93
41	2.42	55.58	2.42	44.29	30.68	44.30	0.99	0.87	0.99	0.96	4.99	0.96
51	2.61	57.13	2.61	43.97	30.56	43.97	0.99	0.86	0.99	1.00	5.03	1.00
61	2.73	55.64	2.73	43.77	30.68	43.77	0.99	0.87	0.99	1.03	5.00	1.03
71	2.82	57.39	2.82	43.62	30.54	43.62	0.99	0.87	0.99	1.04	5.04	1.04
81	2.94	57.44	2.94	43.45	30.54	43.45	0.98	0.86	0.98	1.06	5.07	1.06
91	3.02	60.61	3.02	43.33	30.31	43.33	0.98	0.86	0.98	1.08	5.18	1.08
101	3.12	60.33	3.12	43.19	30.33	43.19	0.98	0.86	0.98	1.09	5.16	1.09
111	3.27	59.58	3.27	42.98	30.38	42.98	0.98	0.86	0.98	1.12	5.17	1.12
121	3.39	60.25	3.39	42.82	30.33	42.82	0.98	0.86	0.98	1.14	5.17	1.14
131	3.49	59.95	3.49	42.71	30.35	42.71	0.98	0.86	0.98	1.15	5.17	1.15
141	3.56	59.95	3.56	42.62	30.35	42.62	0.98	0.86	0.98	1.15	5.17	1.15
150	3.64	59.32	3.64	42.52	30.40	42.52	0.98	0.86	0.98	1.16	5.15	1.16

Table 14: Video quality measures on H 264 decoder without deblocking filter for encoded stream akiyo

Frame number	MSE			PSNR			SSIM			MSAD		
	TI	ARM	P4	TI	ARM	P4	TI	ARM	P4	TI	ARM	P4
1	17.19	55.57	55.57	35.77	30.68	30.68	0.93	0.87	0.87	2.99	4.99	4.99
11	19.52	56.47	58.82	35.23	30.61	30.43	0.94	0.87	0.87	3. 08	5.01	5.08
21	20.74	55.57	60.50	34.96	30.68	30.31	0.94	0.87	0.87	3.16	4.99	5.11
31	20.24	56.47	59.80	35.07	30.61	30.36	0.94	0.87	0.86	3.11	5.01	5.09
41	21.32	55.57	59.83	34.84	30.68	30.36	0.93	0.87	0.86	3.20	4.99	5.10
51	19.97	56.47	63.00	35.13	30.61	30.14	0.94	0.87	0.86	3.13	5.01	5.22
61	21.25	55.57	63.42	34.85	30.68	30.11	0.93	0.87	0.86	3.19	4.99	5.23
71	21.16	56.47	61.72	34.91	30.61	30.22	0.93	0.87	0.86	3.18	5.01	5.17

Table 15: Video quality measures with and without deblocking filter for akiyo

parameters	With deblocking filter			Without deblocking filter		
	TI DSP	ARM	P4	TI DSP	ARM	P4
MSE	2.8	57.4	2.8	20.24	55.96	60.8
PSNR	43.75	30.55	43.75	35.07	30.65	30.29
SSIM	0.986	0.87	0.986	0.94	0.873	0.866
MSAD	1.03	5.065	1.03	3.136	5.0	5.14

The H.264 decoder is implemented on ARM9, TMS320DM642 and Pentium 4 processor. Various parameters such as PSNR, SSIM, MSAD and MSE are calculated for the different video sequences on the three processors. From tables, TI DSP performs better than the other processors for implementing H.264 decoder without deblocking filter than any other processors. Also the decoding time for TI processor is less compared to other processors considered

REFERENCES

[1] V. Lappalainen, A. Hallapuro, T. D. Hämäläinen,"Complexity of Optimized H.26L Video Decoder Implementation," IEEE Trans. Circ and Syst. for Video Technol., vol. 13, pp. 717-725, July 2003.

[2] M. Horowitz, A. Joch, F. Kossentini, "H.264/ AVC Basline Profile Decoder Complexity Analysis," IEEE Trans. Circ. and Syst. Video Technol., vol. 13, pp. 704-716, July 2003.

[3] X. Zhou, E. Q. Li, Y. K. Chen, “Implementation of H.264 Decoder on General-Purpose Processors with Media Instructions,”

SPIE Conf. on Image and Video Comm. and Process., vol. 5022, pp. 224-235, May 2003.

[4] T.T. Shih, C.L. Yang, Y.S. Tung, "Workload Characterization of the H.264/AVC Decoder," Proc. 5th IEEE Pacific-Rim Conf. Multimedia, Japan, November 2004, pp. 957-966.

[5]Thomas Wiegand, Gary Sullivan, Ajay Luthra. Overview of the H.264/AVC Video Coding Standard: IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, VOL. 13, NO. 7, JULY 2003

[6] Document JVT-G050r1, May 2003 http://www.stewe.org/itu-recs/h264.pdf

[7] http://www.vcodex.com/h264.html - Overview of H.264

[8]ARM9TDMI – Technical Reference Manual- www.arm.com

[9]Multimedia communications: applications, networks, protocols and standards By Fred Halsall, Pearson Ed. 2002

[10] Implementation of Context Adaptive Variable Length Coder for H.264 Video Encode International Journal of Recent Trends in Engineering, Vol 2, No. 5, November 2009

[11] H.264: International Telecommunication Union, "Recommendation ITU-T H.264: Advanced Video Coding for Generic Audiovisual Services," ITU-T, 2007

[12] Low-Complexity Transform and Quantization in H.264/AVC IEEE transactions on circuits and systems for video technology, vol. 13, no. 7, july 2003

[13]Adaptive Deblocking Filter IEEE transactions on circuits and systems for video technology, vol. 13, no. 7, July 2003

[14] Ian Richardson 4X4 Transform and Quantization in H.264/ AVC, Vcodex Limited, White Paper, April 200,http://www.vcodex.com/

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