Direct Processor Access for Non Dedicated Server using Multi Core Processor

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Abstract - **The objective of the paper is to design a co processor for a desktop machine which enables the machine to act as non dedicated server, such that the co processor will act as a server processor and the multi-core processor to act as desktop processor. By implementing this methodology a client machine can be made to act as a non dedicated server and a client machine. This type of machine can be used in autonomy networks. This design will lead to design of a cost effective server and machine which can parallel act as a non dedicated server and a client machine or it can be made to switch and act as client or server.**

*Keywords–**Co-Processor,Benchmark Programs, DSP Processor,* **Array Processor.**

I. INTRODUCTION

Multi-core processor is an efficient processor which is widely used for processing digital values to make the processor to perform as client and server in a parallel manner ,a study has been made to about the multi-core processors performance with different benchmark programs and methodologies were worked to identify an efficient processor for network benchmark programs .It is observed that though multi-core is an efficient processor it does not process all the benchmark programs with equal efficiency in that case the processor efficiency is tabulated for all types of benchmark programs .

The best suitable processor for network benchmark program is been enumerated by making network benchmark program to execute in many processor and its also compared with the efficiency of multi-core processor.

*A **Multi-core Processor Performance with Network Benchmark Programs***

To enumerate the performance of different processor with network benchmark programs. As a first step network benchmark program of different capacity is taken, the program is made to execute in a Multi core processor and the time to execute the program is noted down programs. This will give a clear Idea about which programs are to be routed to which co processor while the processor is performing as a desktop machine.

As a first step the performance of Different Benchmark programs are analyzed using multi core processor which acts as main processor the results are compared with the results obtained when same programs are executed with other processor .

Table 1 Performance of Processor using Networking Benchmark Programs using Multi core Processor

Program Specification	**Physical capacity of program**	**Time consumption in seconds**
Network Benchmark	1.2GB	0.64
Network Benchmark	1.14 GB	0.52
Network Benchmark	1.10 GB	0.53
Network Benchmark	1.04 GB	0.60
Network Benchmark	1. GB	0.62
Network Benchmark	850 MB	0.64
Network Benchmark	780MB	0.95

These are the results evolved when network programs are executed using Multi core processor as the next step the same benchmark programs were made to execute using FPGA processor and the readings were tabulated and compared with the readings produced by multi core processor.

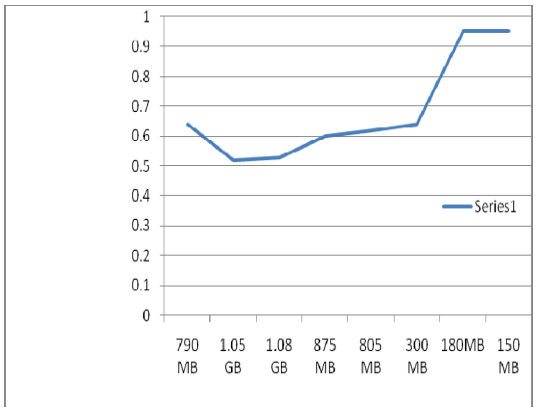

Figure 1: Program Size with respect to time consumption in seconds to execute Network Benchmark program by using multi core processor

The graph will give a clear idea about the time consumption by multi core processor while executing document and network benchmark programs.

B ***Performance of DSP processor for Network Benchmark Programs***

The performance of DSP processor in particular with Network Benchmark program is enumerated. Different network benchmark program are taken and made to execute with a DSP processor and the time Consumed to perform the operation is tabulated

Table 2 Performance of Network Benchmark Programs in DSP Processor

Program Specification	**Program Size**	**Time consumption in seconds with DSP**
Network Benchmark	1.2GB	0.69
Network Benchmark	1.14 GB	0.62
Network Benchmark	1.10 GB	0.63
Network Benchmark	1.04 GB	0.56
Network Benchmark	1. GB	0.51
Network Benchmark	850 MB	0.51
Network Benchmark	780MB	0.5

Using the above values a graph is been plotted between program size and the time consumed to process it by multi core processor and in the same manner graph is plotted for the program size and processing speed by using Digital signal processor.

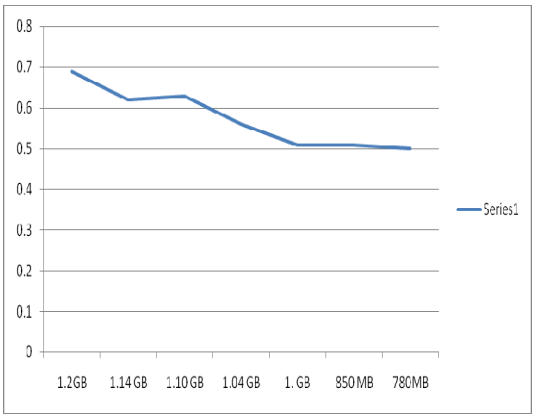

Figure 2: Program Size with respect to time consumption in seconds to execute Network Benchmark program by using DSP processor

C ***Performance Comparison with Networking Benchmark Programs***

The same process of testing can be carried out with networking benchmark programs to analyze the performance of FPGA processor with networking Benchmark programs.

Table 3 Performance of Network Benchmark Programs in Multicore Processor and FPGA Processor

Program Specification	**Program Size**	**Time consumption in seconds with Multi-core processor**	**Time consumption in seconds with FPGA processor**
Network Benchmark	790 MB	0.64	0.62
Network Benchmark	1.05 GB	0.52	0.47
Network Benchmark	1.08 GB	0.53	0.50
Network Benchmark	875 MB	0.60	0.57
Network Benchmark	805 MB	0.62	0.60

To analyze the performance of FPGA with network Benchmark programs different programs are made to run in multi-core processor and FPGA processor and the time consumed to process is tabulated.

Figure 3: Program Size with respect to time consumption in seconds to execute Network Benchmark program by using multi core processor and FPGA processor

Using the same procedure both the processor is been tested for document benchmark programs and the results are tabulated and also a graph is drawn to analyze the perfomance

Table 4: Performance of Document Benchmark Programs in Multicore Processor and FPGA Processor

Program Specification	Program Size	Time consumption in seconds with Multicore processor	Time consumption in seconds with FPGA processor
Document Bench	300 MB	0.99	0.84
Document Bench	180MB	0.95	0.81
Document Bench	150 MB	0.95	0.8
Document Bench	100 MB	0.86	0.74
Document Bench	80MB	0.85	0.74

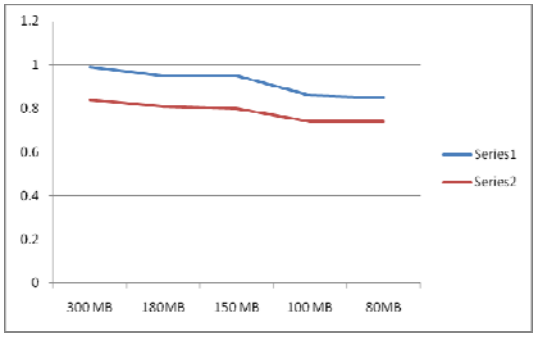

Figure 4: Program Size with respect to time consumption in seconds to execute Document Benchmark program by using multi core processor and FPGA processor

Analysing the perfomance for both the processor in graphical and desktop benchmark programs the FPGA processor performs better than multi core processor in terms of time cosumption.

II. DIRECT PROCESSOR ACCESS DESIGN

With the above readings we have designed a new methodology Direct Processor access.In this methodology a FPGA and a DSP will be connected to the Multi Core Processor as Co Processor . Using this when the non dedicated server is made to perform as client machine the Multi core processor will be processing the data . When the machine is made to act as server in non dedicated manner the multicore processor will be made to act as server and process the data. When any data has to be processed by the user those processing will be made to process by the co – processor. By applying this methodology the non dedicated server can be made to work with parallel efficient to dedicated server.

CONCLUSION

By implementing Direct process access a non dedicated server can be made to work inline with a dedicated server .This will result in effective resource utilizing, cost effective ness and optimization .

REFERENCES

[1] E. Rohou and M. Smith, (1999), "Dynamically managing processor temperature and power," *Proc. FDDO-2*

[2] S. I. Souri, K. Banerjee, A. Mehrotra, and K. C. Saraswat,(2000) "Multiple Si layer ICs: Motivation, performance analysis, and design implications," *Proc Design Automation Conf.*, pp. 873-880.

[3] S. Das, A. Chadrakasan, (2003) "Three-dimensional integrated circuits: performance, design methodology, and CAD tools," *Proc. IEEE Annual Symp. on VLSI*,pp. 13-18.

[4] M.B. Kleiner, S. A. Kuhn, P. Ramm and W. Weber,(1995) "Thermal analysis of vertically integrated circuits." *Tech. Dig. Int'l Electron Devices Meeting*, pp.487-490.

[5] A. Rahman, R. Reif, (2001) "Thermal analysis of three dimensional (3-D) integrated circuits (ICs)," *Proc.Int'l Interconnect Technology Conf.*, pp. 157-159.

[6] F. Fallah and M. Pedram,(2005) "Standby and active leakage current control and minimization in CMOS VLSI circuits." *IEICE Trans. on Electronics*, Special Section on Low-Power LSI and Low-Power IP, Vol. E88-C, No. 4, pp. 509-519.

[7] B. Chatterjee, M. Sachdev, S. Hsu, R. Krishnamurthy, and S. Borkar, (2003) "Effectiveness and scaling trends of leakage control techniques for sub-100nm CMOS technologies," *Proc. Int'l Symp. Low-power Electronics*, pp. 122-127.

[8] M.L. Mui, K. Banerjee, A. Mehrota, (2004) "Power supply optimization in sub-130nm leakage dominant technologies," *Proc. Int'l Symp. Quality Electronic Design*, pp. 409-414.

[9] *Int'l Technology Roadmap for Semiconductors* (ITRS), 2004.

[10] K. Banerjee, A. Mehrotra, A. Sangiovanni- Vincentelli, and C. Hu (1999) "On Thermal Effects in Deep Sub-Micron VLSl Interconnects," *Proc. Design Automation Conf.* , pp. 885-891.

[11] H. J. M. Veendrick (1984) "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," *IEEE Journal of Solid-State Circuits*, vol. 19, pp. 468–473.

[12] A. Alvandpour, P.L. Edefors, C. Svensson, (1998) "Separation and extraction of short-circuit power consumption in digital CMOS VLSI circuits," *Proc. Low Power Electronics and Design*, pp. 245-249.

[13] S. Turgis, N. Azemard, and D. Auvergne, (1996) "Explicit evaluation of short-circuit power dissipation and its influence on propagating delay for static CMOS gates," *Proc. IEEE Int. Symp. on Circuits and Systems,*vol. 4, pp. 751-754.
[14] S.H. Jung, J.H. Baek, S.Y. Kim, (2001) "Short circuit power estimation of static CMOS circuits," *Proc. Asia- Pacific Design Automation Conf.*, pp. 545-549.
[15] P.S.Balamurugan, K.Thanushkodi, (2009) "Array Cache An Efficient Memory For Multi Core Processor", Kyoto Journal of Engineering Research, Vol XI, 0024-609X

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