A BICS Design to Detect Soft Error in CMOS SRAM

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***Abstract*—This paper presents a Built In Current Sensor (BICS) design to detect soft error under both standby and operating condition in Complementary Metal Oxide Semiconductor (CMOS) Static Random Access Memory (SRAM). BICS connected in each column of SRAM cell array detects various values of current signal generated by particle strike. The generated current value is then compared with the reference value. An error signal is generated when it exceeds the reference value. The existing Built In Current Sensors are used to detect the soft error only at the time of standby condition. But there is a possibility of occurrence of soft error during operation conditions also. During write operation, the soft error occurs at the time of end of the write cycle. But in read operation the error can occur at any instant of time. Hence a BICS is designed in such a way that it can monitor the occurrence of soft error at any time instant of the operating condition as well as stand by condition.**

Keywors - BICS; soft error; SRAM;

I. INTRODUCTION

Semiconductor memories are moving towards higher levels of integration. This increase in integration is achieved through reduction in storage cell size causing a reduction in the charge representing a stored bit. This raises the reliability issues of memories [1]. Moreover, memories occupy the largest area in modern ICs. Hence the drastic device shrinking with higher operating speeds reduce the reliability of deep submicron ICs. When memories (SRAM) are used in critical applications like space, the main cause for reliability reduction is due to soft errors also called as single event upsets (SEUs), which are radiation-induced transient errors caused by neutrons from cosmic rays and alpha particles from packaging materials. Errors occurring in SRAMs can be hard and soft (transient) errors. Hard errors are the permanent faults that cannot be overcome by rewrite operation. Structured scan-based and BIST techniques are effective means to detect permanent faults [2]. However, soft errors are due to heavy particles incident on sensitive node of the SRAM producing electron-hole pairs, and this ionization can cause flip on data [3, 4]. Thus, soft error is a potential threat to the reliability of memories in space environment [5, 6]. Traditionally soft errors were regarded as a major concern only for space applications. But for designs manufactured at deep sub micron technology, soft errors are more frequent due to the alpha particles created by unstable isotopes found in the packaging materials of a chip. Hence soft errors occur not only at space environment, but also occur at the ground level [7, 8]. Thus designing soft error tolerant SRAM is the only way to progress towards technology scaling. Soft errors can be overcome by various methods such as hardening, protection and recovery. Hardening technique uses insertion of transistors like duplicating, to make the cell insensitive to single event upsets [9]. The main drawback of the work done in [9] is, it uses 12 transistors for each memory cell, increasing the area by twice. Protection method uses capacitor, which is vertically connected between two storage nodes (Q, Qbar) of SRAM cell [10]. When particle due to radiation, strikes on sensitive node of the SRAM cell, the capacitor gets charged. But this method is applicable only for stand by condition and if we use this capacitor for operating condition, it will increase the access time. Recovery method uses error detection and correction principle. To maintain the acceptable reliability levels of SRAM, Error Correcting Codes (ECC) are often used to detect and correct soft errors often called as SEU. But ECC may cause area overhead, and significant performance and power dissipation. This technique detects and corrects the error only while reading the faulty bit. So there will be latency between the occurrence of the SEU and correction, which can cause accumulation of SEUs.

These drawbacks can be overcome by using BICS to detect soft errors. Traditional BICS [11, 12, 13, and 14] are used to monitor the static current dissipation on the circuit, which is synchronous in nature. On the other hand SEU can occur at any instant of time. To cope with these problem asynchronous BICS are used [15], which has asynchronous latch. This BICS is connected on the vertical power lines of a memory to find the faulty column. Parity bit per memory word was used to find the faulty row, in such a way that it can detect the affected bit and will perform the error correction. The BICS used is asynchronous one. This makes the BICS design more difficult than synchronous BICS. The BICS in [16] has more voltage drop in Vdd and gnd. It is overcome by BICS in [17], where only single cell is considered for a column which results in the voltage drop of less than 10mV. But the BICS in [17] cannot detect the soft error under operating condition.

The aim of this paper is to propose a BICS, which detects the soft error under both operating and standby condition without affecting the performance of the BICS as in [17]. All the simulations have been carried out using T-spice in 90 nm technology.

This paper is organized as follows. Section II discusses about the radiation effect on SRAM cell. SRAM soft error is explained in Section III. Section IV discusses about existing BICS [17] and the proposed BICS circuit is described in

Section V. Section VI discusses about the simulation results obtained and finally some conclusions are offered.

II. RADIATION EFFECT ON SRAM CELL

A. *Sources of Radiation*

Memory performances are severely affected by the radiation particles. These charge particles are present in the space environment as cosmic rays and they are present within the chip as α-particles. The α-particle is caused by the radioactive decay of uranium and thorium impurities present in the chip packaging materials and interconnects of the chip.

B. *Single Event Upset in SRAM*

Single Event Upset (SEU) in memories refers to the loss of information from a memory cell caused by a single ionizing particle. The effect of SEU in a SRAM cell is the flip of data from 0 to 1 or 1 to 0 and is reversible. The correct data can be rewritten. When a single high energy particle strikes the sensitive nodes of the SRAM cell, the charge generation and collection occurs as shown in Figure 1. The two sensitive nodes in the SRAM cell are the drain of the OFF_NMOS and the drain of the OFF_PMOS. The drain of the OFF-MOS transistors forms the reverse biased PN junctions with the substrates. These junctions are more sensitive to particle strikes and will cause the generation of electrons and hole pairs, when the particle passes through the PN junction. The generated electrons move towards the positive voltage of reverse biased junction and holes move toward the negative voltage side. These movement of charges cause the generation of current pulse at the sensitive nodes of the cell. The memory cell flips the data when collected charge exceeds the critical charge (Q_{crit}) that has been stored in the sensitive node, where the critical charge Q_{crit} is the minimum charge required to flip the data.

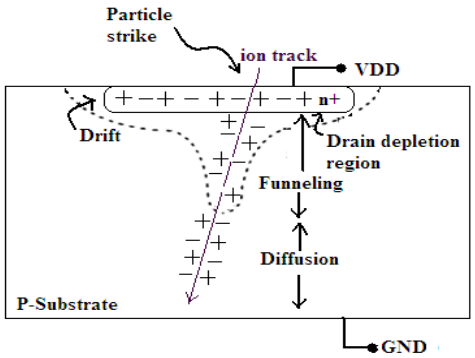

Figure 1: Particle strike and charge generation

The critical charge not only depends on the charges collected at the struck node, but also depends on the current pulse produced at the same node. This current pulse is equivalent to the current between drain and the substrate.

III. SRAM SOFT ERROR

In CMOS circuits SEUs are modeled by injecting the current pulses at the sensitive nodes. The current pulse has fast rise time and gradual fall time. The shape of current pulse is approximated by (1)

$$I_\alpha(t) = \frac{Q}{t_f - t_r}\left(e^{\frac{-t}{t_f}} - e^{\frac{-t}{t_r}}\right) \qquad (1)$$

where Q is the charge collected due to particle strike, t_r is the rise time and t_f is the fall time. Figure 2 shows the conventional 6T SRAM cell designed at 90 nm process technology with operating voltage of 1.05 V having two sensitive nodes Q and QBAR.

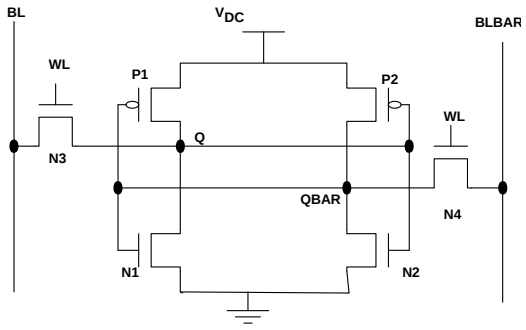

Figure 2: Conventional 6T SRAM cell

A. *Soft error under stand by condition*

The soft error can occur at any instant of time, when the SRAM is under standby condition. At standby condition, a 1 to 0 flip is said to occur when the particle strikes and discharges the charge stored at the drain of the OFF-NMOS transistor. Similarly a 0 to 1 flip is said to occur when the particle strikes and discharges the drain of the OFF-PMOS transistor.

For analysis, the current pulse with t_r = 5 ps and t_f = 370 ps is injected at the OFF-NMOS transistor (N1) of the SRAM cell shown in figure 2. Figure 3 shows the simulation result of SRAM cell soft error under standby condition. From 0 to 10 ns word line (WL) is enabled during which bit line (BL) remains high and Bit line bar (BLBAR) remains at 0. Hence the node Q has the value 1 and QBAR 0 as shown. At 15 ns when the current pulse is injected at node Q the data gets flipped from 1 to 0 at node Q and from 0 to 1 at node QBAR indicating the occurrence of soft error.

B. *Soft error under operating condition*

Figure 4, 5 and 6 indicates the occurrence of soft error under operating conditions. Figure 4 shows that the data flip does not occur when the current pulse is injected at the intermediate time of write operation (5 ns). Figure 5 shows that the data gets flipped when current pulse is injected at the end of write operation (9.7 ns). Figure 6 shows the flip of data when the current pulse is injected during read cycle (15 ns).

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Table I and II shows the various simulations done at the end of write cycle and during read cycle respectively, for different charge and different fall time where as the rise time is constant as 10ps. From table I and II, it is found that the BICS detects the error at the time of no flip condition also; this is to make sure that the BICS does not leave any soft error undetected.

TABLE I. SIMULATION RESULTS FOR WRITE TIME SOFT ERROR

Charge Q (pC)	Delay time tf (ps)				
	100	*200*	*300*	*400*	*500*
2.0	F, D	F, D	NF, D	NF, ND	NF, ND
2.5	F, D	F, D	F, D	NF, D	NF, ND
3.0	F, D	F, D	F, D	F, D	NF, D

TABLE II. SIMULATION RESULTS FOR READ TIME SOFT ERROR

Charge Q (pC)	Delay time tf (ps)				
	100	*200*	*300*	*400*	*500*
0.25	F, D	NF, D	NF, D	NF, ND	NF, ND
0.5	F, D	F, D	F, D	NF, D	NF, ND
0.75	F, D	F, D	F, D	F, D	NF, D

Where F, D - flip and detected.
NF, D - No flip but detected.
NF, ND - No flip and no detection.

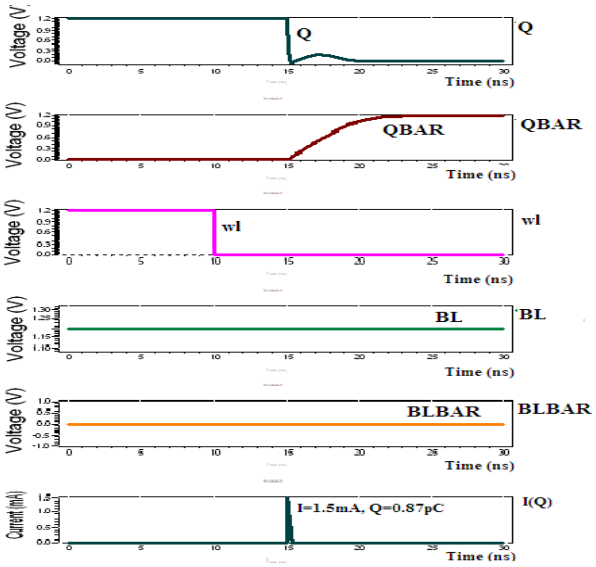

Figure 3: SRAM soft error under standby condition

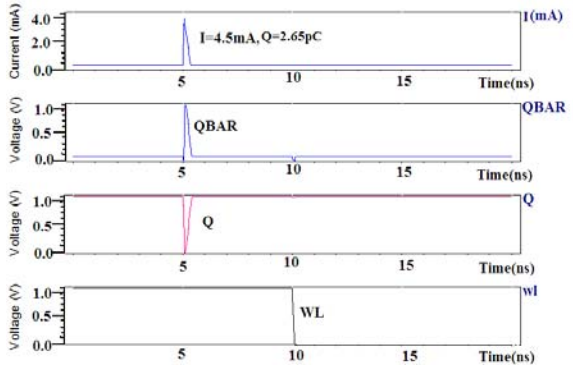

Figure 4: No flip under intermediate time of write operation

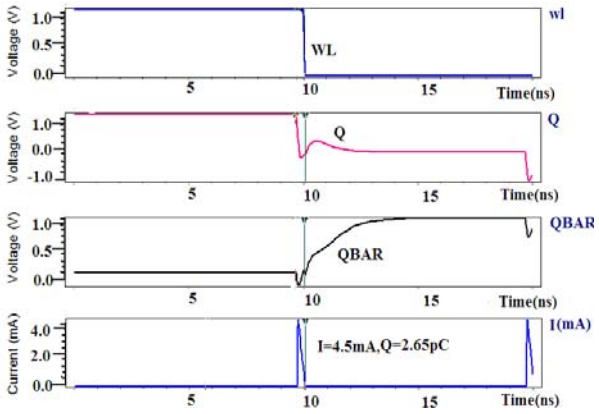

Figure 5: Flip at the end of write operation

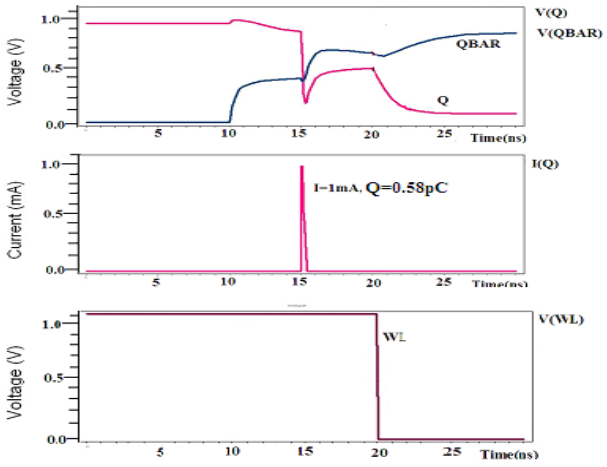

Figure 6: Data flip during read operation

IV. EXISTING BUILT IN CURRRENT SENSOR

Figure 7 shows the BICS used in [17]. It uses two comparators and one asynchronous latch. Each comparator has current mirror and one current source inverter. The current mirror is used to amplify the upset current, and this amplified current pulse is converted into logic level voltage by current source inverter. In figure 7, S_{vdd} is a 1 to 0 flip detector to observe 1 to 0 flip due to radiation, and S_{gnd} is used to detect 0

to 1 flip. Both S_{vdd} and S_{gnd} provide logic level voltage pulses when flip occurs.

These outputs are connected to the asynchronous latch. If any of the two outputs goes high then the latch is triggered and it gives the error signal Err_1 as high. The reset signal (RST) is used to reset the asynchronous latch, after the upset is detected and during write and read operation. The BICS provides vdd' and gnd' to the column of the SRAM array. The reference voltage generator is used to give the biasing voltage $B_{v,}$ B_g for S_{vdd} and S_{gnd}. This BICS is capable of detecting soft error only during standby condition but figure 5 and figure 6 indicates the occurrence of soft error during operating conditions also. Hence, a novel BICS is proposed which is capable of detecting soft error at both standby and operating conditions.

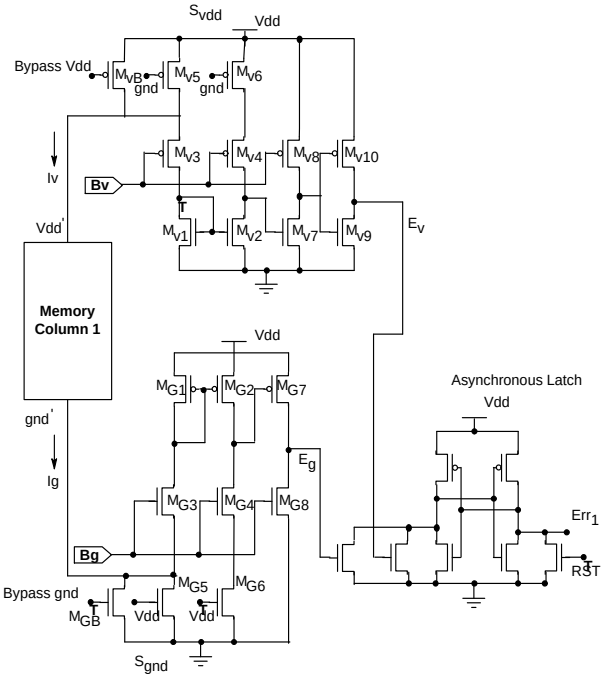

Figure 7: Existing BICS

V. PROPOSED BUILT IN CURRRENT SENSOR

Figure 8 shows the proposed BICS. It uses two comparators and one asynchronous latch. Each comparator has current mirror and one current source load inverter. Transistors T_1 to T_8 forms the S_{vdd} part where T_1, T_2 is acting as current mirror and T_7, T_8 acts as current source load inverter. The transistors T5, T6 are source resistor to the current mirror. The source current for both current mirror and inverter is provided by transistors T_3, T_4 and T_8. These three transistors are biased by reference voltage B_v. Similarly M_1 to M_8 forms the S_{gnd} part with B_g as reference voltage, and the signals $Bypass_{vdd}$ and $Bypass_{gnd}$ are used to bypass vdd_i and gnd_i to the memory column of BICS during read and write cycle of the memory.

To enable the BICS operation under operating condition the logic circuitry with delay element is used. This circuit is used to control the reset signal for all operating conditions. The reset control circuit contains one delay element and the transistors R_{p1}, R_{p2}, R_{n1}, R_{n2} and R_3 as shown in figure 8. The input to the delay element is word line (WL) signal. The delay element delays the WL signal when it is enabled during write operation. Buffer is used as the delay element and the buffer is designed to have the required delay. In our case write time is 10 ns, so the required delay is considered as 8.5 ns. The buffer is designed to obtain 8.5 ns delay in such a way that the reset signal is enabled for first 8.5 ns during write operation. The delayed signal is then given to the transistors R_{p2}, R_{n2} and the WL signal is given to transistors R_{p1}, R_{n1}. Similarly read enable signal (Read) is connected to the gate of the transistor R_3.

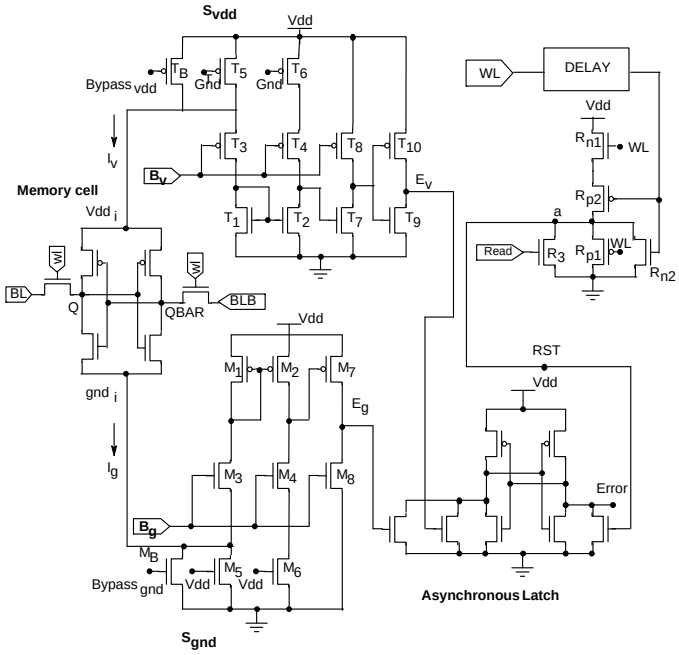

Figure 8: Proposed BICS

During stand by condition WL is in logic 0, R_{p1} is ON, so node 'a' gets discharged and reset signal goes to logic 0 and BICS will be in operation. Hence if any flip occurs error signal will be generated. During read operation, in addition to WL signal, read enable signal (Read) is also enabled so transistor R_3 is switched ON, node 'a' gets discharged and reset signal becomes logic 0 enabling the BICS to generate error signal. Similarly during write operation, WL signal is high and the delayed output is low for first 8.5 ns, turning ON the transistors R_{n1} and R_{p2}. Thus node 'a' remains at VDD, reset signal is in logic 1 disabling BICS for first 8.5 ns. After a delay of 8.5 ns the delayed WL signal remaining high, turns OFF the transistor R_{p2} and turns ON R_{n2}. Thus node 'a' gets discharged making the reset signal low and enables the BICS operation at the end of write cycle (last 1.5 ns). So BICS is

ON for the entire period of standby condition, read operation and at the end of the write operation.

Since there are three different cases as standby, write and read conditions, three different reference voltages are used to determine the BICS sensitivity. The three reference voltages given to B_v is used to compare the voltage drop on line vdd_i to detect 1 to 0 flip. Similarly reference voltages B_g is used to compare the voltage on line gnd_i to detect 0 to 1 flip. The different reference voltages used are given in table III.

TABLE III. BICS REFERENCE VOLTAGES

Condition	Reference voltage in volts	
	Bv	***Bg***
Standby	0.5	0.7
Write operation	0.4	0.8
Read operation	0.6	0.5

When a particle strikes the drain of the OFF NMOS transistor of the SRAM cell the transient current pulse is produced at the struck node. The current flowing from V_{dd} to the struck node through the ON PMOS transistor is I_v. When I_v flows from V_{DD} to the struck node, the current through T1 is reduced and hence the current through T_2 also get reduced. This causes an increase in the voltage drop from the drain to source of the transistor T_2. The drain of the transistor T_2 is connected to the gate of the transistor T_7 and hence increases the gate to source voltage of T_7. This increased gate to source voltage produces a voltage pulse at the drain of T_7. This voltage pulse is amplified and inverted to get full logic value at node E_v by using the transistors T_9 and T_{10}. Similarly S_{gnd} produces the voltage drop at node E_g, when particle strikes at the drain of the OFF PMOS transistor of the cell. The outputs E_v and E_g are the inputs to the asynchronous latch. If any of the two outputs goes high then the latch is triggered and it will generate the error signal (Error) high.

VI. SIMULATION RESULTS AND DISCUSSION

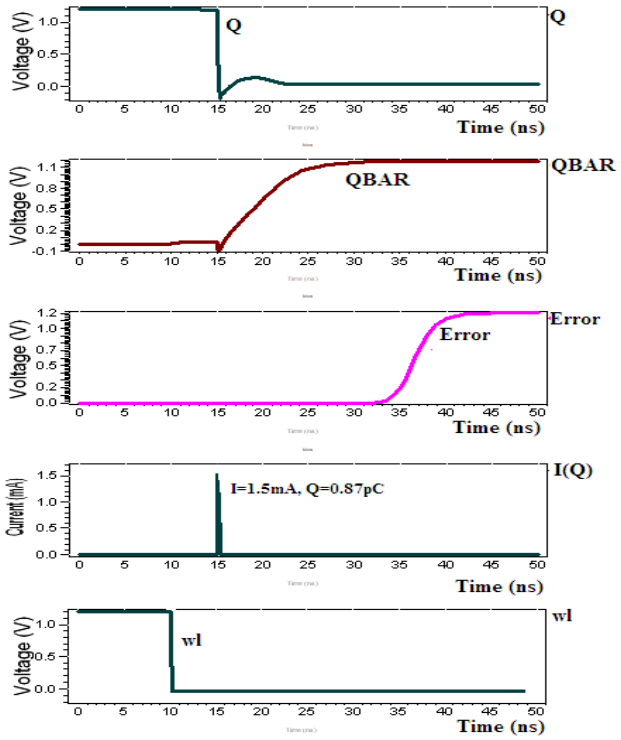

Figure 9: BICS detection of soft error under standby condition

Figure 9 shows the simulation result of the proposed BICS during standby condition. WL signal remains high for 10 ns during which data 1 is written into the cell making the node Q high. When the current pulse (I) is injected at 15 ns the data gets flipped (Q becomes 0 and QBAR becomes 1). This upset is detected by BICS and makes the error signal (Err1) high.

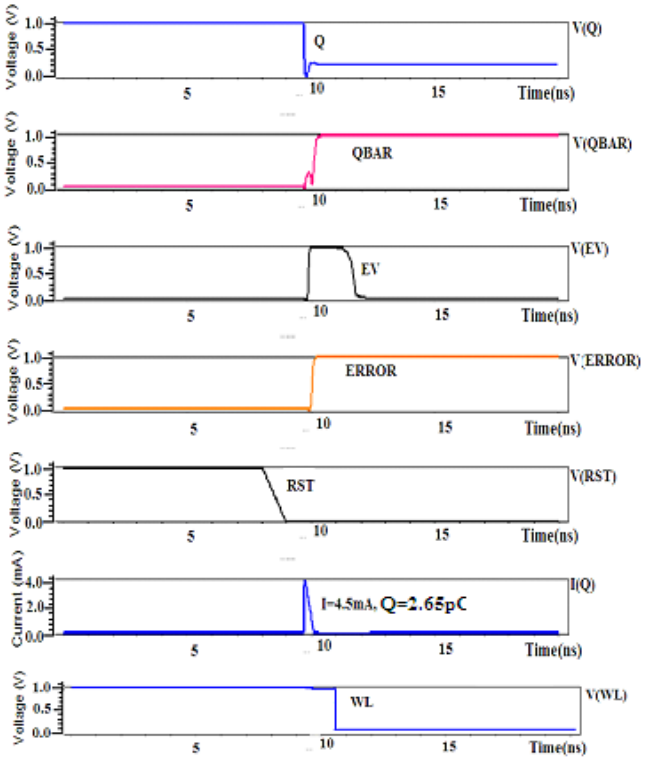

Figure 10: BICS detection of soft error at the end of write cycle

Figure 10 shows the simulation result of 1 to 0 flip at the end of write operation. The current pulse is generated by using (1) with Q = 2.65 pC, t_f = 370 ps and t_r = 10 ps. WL signal remains high for 10 ns during which data 1 is written into the cell making the node Q high. When the current pulse (I(Q)) is injected at 9.3 ns the data gets flipped (Q becomes 0 and QBAR becomes 1). The signal EV is one of the inputs to the asynchronous latch to generate the error signal (ERROR). The signal RST becomes low after 8.5 ns during which the error signal is generated at the end of write operation.

Figure 11 shows the simulation result of 1 to 0 flip during the read cycle. The current pulse is generated using (1) with Q=.58 pC, The first chart in figure 11 shows the 1 to 0 and 0 to 1 data flip of Q and QBAR respectively. The second chart shows the current pulse generation using (1) for the charge of Q=.58 pC, t_f = 370 ps and t_r = 10 ps. Fourth chart shows the signal Ev which is the input to the asynchronous latch and the last chart shows the error signal generated due to soft error during the read cycle when WL signal remains high.

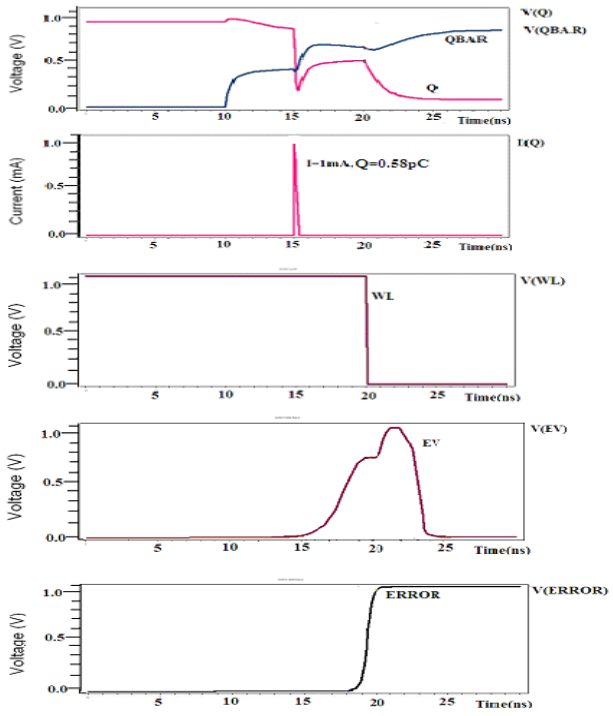

Figure 11: BICS detection of soft error during read cycle

CONCLUSION

In this paper, we have proposed a BICS Design, capable of detecting soft errors during standby and operating condition. Simulation results clearly indicate the occurrence of soft error at the end of write cycle and at the intermediate time of read cycle in addition to standby condition. The proposed BICS design with a delay block and internal reset signal generation is capable of turning ON the BICS during the required operating conditions. This makes possible the detection of soft error at any instant of time of its occurrence irrespective of standby or operating condition.

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